ST7701S

Datasheet

Version 1.1

2017/04

Sitronix Technology Corporation

LIST OF CONTENT

1 GENERAL DESCRIPTION

The ST7701S, a 16.7M-color System-on-Chip (SOC) driver LSI designed for small and medium sizes of TFT LCD display, is capable of supporting up to 480RGBX864 in resolution which can transmit graphic data without RAM. The 480-channel source driver has true 8-bit resolution, which generates 256 Gamma-corrected values by an internal D/A converter.

The ST7701S is able to operate with low IO interface power supply and incorporate with several charge pumps to generate various voltage levels that form an on-chip power management system for gate driver and source driver.

The built-in timing controller in ST7701S can support several interfaces for the diverse request of medium or small size portable display.ST7701S provides several system interfaces ,which include MIPI/RGB/SPI.For further power control ,the dynamic backlight control function basing on displaying image content is also supported.

2 FEATURES

- Single chip WVGA a-Si TFT-LCD Controller/Driver without Display RAM
- Display Resolution
  - 480*RGB (H) *864(V) (WVGA)
  - 480*RGB (H) *854(V)
  - 480*RGB (H) *800(V)
  - 480*RGB (H) *720(V)
  - 480*RGB (H) *640(V) (VGA)
  - 480*RGB (H) *360(V)
- LCD Driver Output Circuits
  - Source Outputs: 480 RGB Channels
  - Support gate control signals to gate driver in the panel
  - Common Electrode Output
- Display Colors (Color Mode)
  - Full Color mode : 16.7M-colors, RGB=(888) max., Idle Mode Off
  - Reduce color mode: 262K colors
  - Reduce color mode: 65K colors
  - Idle Mode: 8-color, RGB=(111)
- Programmable Pixel Color Format (Color Depth) for Various Display Data input Format
  - 24-bit/pixel: RGB=(888)
  - 18-bit/pixel: RGB=(666)
  - 16-bit/pixel: RGB=(565)
- Display Interface
  - 8 bit,9bit and 16 bit serial peripheral interface
  - 16/18/24 RGB Interface(VSYNC, HSYNC, DOTCLK, ENABLE, DB[17:0],Sync and DE mode)
  - MIPI Display Serial Interface (DSI V1.01 r11 and D-PHY V1.0, 1 clock and 1 or 2 data lane pairs)

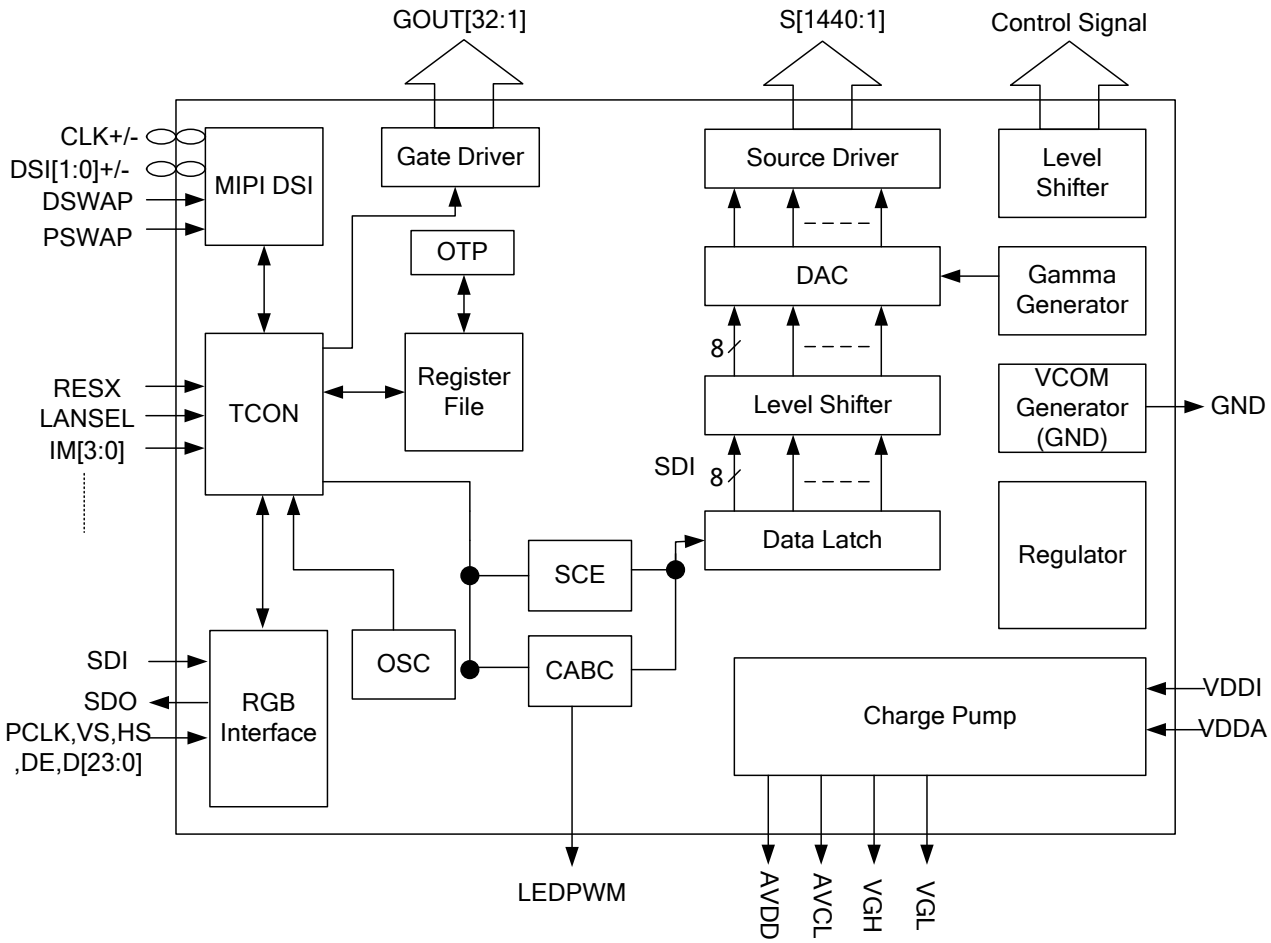
    Supports one data lane / maximum speed 800Mbps

    Supports two data lanes / maximum speed 550Mbps
- Display Features
  - Programmable Partial Display Duty
  - CABC for saving current consumption
  - Color enhancement
- On Chip Build-In Circuits
  - DC/DC Converter
  - Adjustable VCOM Generation
  - Non-Volatile (NV) Memory to Store Initial Register Setting and Factory Default Value (Module ID, Module Version, etc)

- Timing Controller
- 4 preset Gamma curve with separated RGB Gamma setting

- Build-In NV Memory for LCD Initial Register Setting
  - OTP to store VCOM and ID1~ID3
- Driving Algorithm Support
  - 1-dot/2-dot/3-dot/4-dot Inversion
  - Column Inversion
  - Zigzag Inversion
- Wide Supply Voltage Range
  - I/O Voltage (VDDI to DGND): 1.65V ~ 3.3V (VDDI≦ VDD)
  - Analog Voltage (VDDA to AGND): 2.5V ~ 3.6V
  - MIPI Voltage (VDDAM to VSSAM): 2.5V ~ 3.6V
- On-Chip Power System
  - Source Voltage (VAP (GVDD) to VAN (GVCL)): +3.64~6.5V, -1.05~-5V
  - VCOM level: GND
  - Gate driver HIGH level (VGH to AGND): +11.5V ~ +17 V
  - Gate driver LOW level (VGL to AGND): -12V ~ -7.6V
- Optimized layout for COG Assembly
- Operate temperature range: −30℃ to +85℃
- Lower Power Consumption

5 BLOCK DIAGRAM



6 PIN DESCRIPTION

6.1 Power Supply Pins

Name	I/O	Description	Connect Pin
VDDI	I	Power Supply for I/O System.	VDDI
VDDA	I	Power Supply for Analog, Digital System and Booster Circuit.	VDDA
VDDM	I	Power Supply for MIPI Circuit.	VDDA
VDDB	I	Power Supply for internal Circuit.	VDDA
VDDB2	I	Power Supply for internal Circuit.	VDDA
VDDR	I	Power Supply for internal Circuit.	VDDA
VDDR1	I	Power Supply for internal Circuit.	VDDA
VSSB	I	System Ground for internal Circuit.	AGND
VSSB2	I	System Ground for internal Circuit.	AGND
VSSR	I	System Ground for internal Circuit.	AGND
VSSA	I	System Ground for internal Circuit.	AGND
VSSM	I	System Ground for MIPI Circuit.	AGND
SGND	I	System Ground for internal Circuit.	AGND
AGND	I	System Ground for Analog System and Booster Circuit.	AGND
DGND	I	System Ground for I/O System and Digital System.	DGND
VPP	I	When programming NVM, can select internal power or external power supply voltage (7.5V); the current of Ivpp must be more than 10mA. ***If select internal power then leaves the pin open when not in use.***	External Power

6.2 Bus Interface Pins

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Connect Pin</th></tr>
<tr><td colspan="4">Digital Control</td></tr>
<tr><td>IM3, IM2,
IM1, IM0</td><td>I</td><td>-The System interface mode select.

<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU Interface Mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>RGB+8b SPI(fall)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>RGB+9b SPI(fall)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>RGB+16b SPI(rise)</td></tr>
<tr><td>0/1</td><td>1</td><td>0</td><td>1</td><td>MIPI</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>MIPI+16b SPI(rise)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>RGB+8b SPI(rise)</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>RGB+9b SPI(rise)</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>RGB+16b SPI(fall)</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>MIPI+16b SPI(fall)</td></tr>
</table></td><td>VDDI/DGND</td></tr>
<tr><td>RESETSX</td><td>I</td><td>- The external reset input
- Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.</td><td>MPU</td></tr>
<tr><td>NBWSEL</td><td>I</td><td>Input pin to select the gamma voltage level sequence of V0~V255.
Low: V0 > V1 >…> V254 > V255, normally white
High: V255 > V254 >…> V1 > V0, normally black
Fix to VDDI level when not in use.</td><td>VDDI/DGND</td></tr>
<tr><td>GO [3:0]</td><td>O</td><td>General purpose output pins. The output voltage swing is VDDI to DGND.
Leave the pin open.</td><td>MPU
VDDI/DGND</td></tr>
<tr><td colspan="4">SPI Interface</td></tr>
<tr><td>CSX</td><td>I</td><td>- A chip select signal
Low: the chip is selected and accessible
High: the chip is not selected and not accessible
Fix to VDDI or DGND level when not in use.</td><td>MPU</td></tr>
<tr><td>DCX</td><td>I</td><td>- The SPI interface (DCX): The signal for command or parameter select.
Low: Command
High: Parameter
Fix to VDDI or DGND level when not in use.</td><td>MPU</td></tr>
</table>

Name	I/O	Description	Connect Pin
SCL	I	SCL: Serial clock input for SPI interface. ***Fix to VDDI or DGND level when not in use.***	MPU
SDA	I	SDA: Serial data input/output bidirectional pin for SPI Interface. ***Fix to DGND level when not in use.***	MPU
SDO	O	Serial data output pin used for the SPI Interface. ***Leave the pin open when not in use.***	MPU
I2C_SA[0:1]	I	***Fix to VDDI or DGND level.***	MPU
RGB Interface			
PCLK	I	Dot clock signal for RGB interface operation ***Fix to VDDI or DGND level when not in use.***	MPU
VS	I	Frame synchronizing signal for RGB interface operation ***Fix to VDDI or DGND level when not in use.***	MPU
HS	I	Line synchronizing signal for RGB interface operation ***Fix to VDDI or DGND level when not in use.***	MPU
DE	I	Data enable signal for RGB interface operation Low: access enabled High: access inhibited ***Fix to VDDI or DGND level when not in use.***	MPU
DB [23:0]	I/O	A 24-bit parallel data bus for RGB Interface. 24-bit/pixel: D[23:16]=R,D[15:8]=G,D[7:0]=B 18-bit/pixel: MDT=0:D[21:16]=R,D[13:8]=G,D[5:0]=B MDT=1:D[17:12]=R,D[11:6]=G,D[5:0]=B 16-bit/pixel: D[20:16]=R,D[13:8]=G,[4:0]=B ***Fix to VDDI or DGND level when not in use.***	MPU
CABC Control			
LEDON	O	Used for turning On/Off external LED backlight control. ***Leave the pin open when not in use.***	CABC
LEDPWM	O	The PWM frequency output for LCD driver control. ***Leave the pin open when not in use.***	CABC
MIPI Interface			
CP CN	I	MIPI DSI differential clock pair. That the COG resistance is less than 10 ohm. ***If MIPI are not in use, they should be connected to VSSM.***	MIPI
DP0 DN0 DP1	I/O	MIPI DSI differential data pair. That the COG resistance is less than 10 ohm. ***If MIPI are not in use, they should be connected to VSSM***	MIPI

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Connect Pin</th></tr>
<tr><td>DN1</td><td></td><td></td><td></td></tr>
<tr><td>ERR</td><td>O</td><td>CRC and ECC error output pin for the MIPI interface, activated by S/W command. This pin is output low when it is not activated. When this pin is activated, it is output high if CRC/ECC error is found.
Leave the pin open when not in use.</td><td>MIPI</td></tr>
<tr><td>LANSEL</td><td>I</td><td>Input pin to select 1 data lane or 2 data lanes in MIPI/MDDI interface.
Low: 1 data lane
High: 2 data lanes
Fix to VSSI level when not in use.</td><td>MIPI</td></tr>
<tr><td>DSWAP
PSWAP</td><td>I</td><td>Differential clock polarity swap
For MIPI interface
<table>
<tr><th rowspan="2">DSWAP</th><th rowspan="2">PSWAP</th><th colspan="6">Pins</th></tr>
<tr><th>CLK_P</th><th>CLK_N</th><th>D0_P</th><th>D0_N</th><th>D1_P</th><th>D1_N</th></tr>
<tr><td rowspan="2">0</td><td>0</td><td>CLK_P</td><td>CLK_N</td><td>D0_P</td><td>D0_N</td><td>D1_P</td><td>D1_N</td></tr>
<tr><td>1</td><td>CLK_N</td><td>CLK_P</td><td>D0_N</td><td>D0_P</td><td>D1_N</td><td>D1_P</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td>CLK_P</td><td>CLK_N</td><td>D1_P</td><td>D1_N</td><td>D0_P</td><td>D0_N</td></tr>
<tr><td>1</td><td>CLK_N</td><td>CLK_P</td><td>D1_N</td><td>D1_P</td><td>D0_N</td><td>D0_P</td></tr>
</table></td><td>VDDI/DGND</td></tr>
</table>

Note1. "1" = VDDI level, "0" = DGND level.

Note2. When in parallel mode, unused data pins must be connected to "1" or "0".

Note3. When CSX="1", there is no influence to the parallel and serial interface.

6.3 Driver Output Pins

Name	I/O	Description	Connect pin
S [1:1440]	O	Source output voltage signals applied to a LCD panel	LCD
GOUT [1:32]	O	Gate control signals and the swing voltage level is VGHO to VGLO	LCD
SDUM [0:3]	O	Dummy Source ***Leave the pin open when not in use.***	LCD
VCOM	O	Regulator output for common voltage of panel. ***Fix to AGND level.***	LCD
VGL	O	Connect to VGL or OPEN.	LCD
VGHS	O	Connect to VGH.	LCD

6.4 Test and other pins

VCC	O	Used for monitoring.	OPEN
VCCMA	O	Used for monitoring.	OPEN
V20	O	Used for monitoring.	OPEN
VPS1/VPS2	O	Used for monitoring.	OPEN
VCCMD	O	Used for monitoring.	OPEN
V12TX	O	Used for monitoring.	OPEN
AVDD	O	Power Pad for analog Circuit.	OPEN
AVCL	O	Power Pad for analog Circuit.	OPEN
VAN	O	A power output of grayscale voltage.	OPEN
VAP	O	A power output (negative) of gray scale voltage.	OPEN
RDX	I	Input pin for testing. ***Fix to VDDI or DGND level.***	VDDI/DGND
DSTB_SEL	I	input pin for testing. ***Fix to DGND level.***	DGND
EXB1T	I	This pin is for test.. ***Fix to DGND level when not in use.***	DGND
VGSW [0:3]	I	Input pins for testing. ***Fix to DGND level when not in use.***	VDDI/DGND
TESTO [0:3]	O	Output pins for testing. Please keep these pins floating.	OPEN
TE_L	O	For IC Test. ***Leave the pin open when not in use.***	OPEN
VGHP	O	Power Pad for analog Circuit.	OPEN
VGHEQ2	O	Output pins for testing.	OPEN

		Please keep this pin floating.	
VSSIDUM0~3	I	GND Dummy pads. Connect to AGND.	AGND
PADA1 PADB1 PADA2 PADB2	I/O	These test pins for chip attachment detection. PADA1 to PADA2 are output pins and PADB1 to PADB2 are input pins. -For normal operation: Connect PADA1 and PADB1 together by ITO trace. Connect PADA2 and PADB2 together by ITO trace.	OPEN
CNTACT1 CNTACT2	I/O	Test pin , for test bonding quality.	OPEN
DUMMY	-	These pins are dummy (no electrical characteristic) Can pass signal through these pads on TFT panel. Please open these pins.	OPEN

7 DRIVER ELECTRICAL CHARACTERISTICS

7.1 Absolute Operation Range

Item	Symbol	Rating	Unit
Supply Voltage	VDD	- 0.3 ~ +4.6	V
Supply Voltage (Logic)	VDDI	- 0.3 ~ +4.6	V
Driver Supply Voltage	VGH-VGL	-0.3 ~ +30.0	V
Logic Input Voltage Range	VIN	-0.3 ~ VDDI + 0.3	V
Logic Output Voltage Range	VO	-0.3 ~ VDDI + 0.3	V
Operating Temperature Range	TOPR	-30 ~ +85	℃
Storage Temperature Range	TSTG	-40 ~ +125	℃

Table 1 Absolute Operation Range

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

7.2 DC Characteristics

Parameter	Symbol	Condition	Specification			Unit	Related Pins
			MIN.	TYP.	MAX.		
Power & Operation Voltage							
System Voltage	VDD	Operating voltage	2.5	2.8	3.6	V	
Interface Operation Voltage	VDDI	I/O Supply Voltage	1.65	1.8	3.3	V	
Gate Driver High Voltage	VGH		11.5		17	V	
Gate Driver Low Voltage	VGL		-7.6		-12	V	
Gate Driver Supply Voltage		| VGH-VGL |	-		30	V	
Input / Output							
Logic-High Input Voltage	VIH		0.7VDDI		VDDI	V	Note 1
Logic-Low Input Voltage	VIL		VSS		0.3VDDI	V	Note 1
Logic-High Output Voltage	VOH	IOH = -1.0mA	0.8VDDI		VDDI	V	Note 1
Differential Input High Threshold Voltage	VIT+			0	50	mV	MIPI_CLK MIPI_Data
Differential Input Low Threshold Voltage	VIT-		-50	0		mV	
Single-ended Receiver Input Operation Voltage Range	VIR		0.5		1.2	V	
Logic-Low Output Voltage	VOL	IOL = +1.0mA	VSS		0.2VDDI	V	Note 1
Logic-High Input Current	IIH	VIN = VDDI			1	uA	Note 1
Logic-Low Input Current	IIL	VIN = VSS	-1			uA	Note 1
Input Leakage Current	IIL	IOH = -1.0mA	-0.1		0.1	uA	Note 1
VCOM Voltage							
VCOM amplitude	VCOM			VSS		V	
Source Driver							
Gamma Reference Voltage(Positive)	VAP		4.4		6.4	V	
Gamma Reference Voltage(Negative)	VAN		-2.6		-4.6	V	
Source Output Settling Time	Tr	Below with 99% precision			10	us	Note 2

Table 2 Basic DC Characteristics

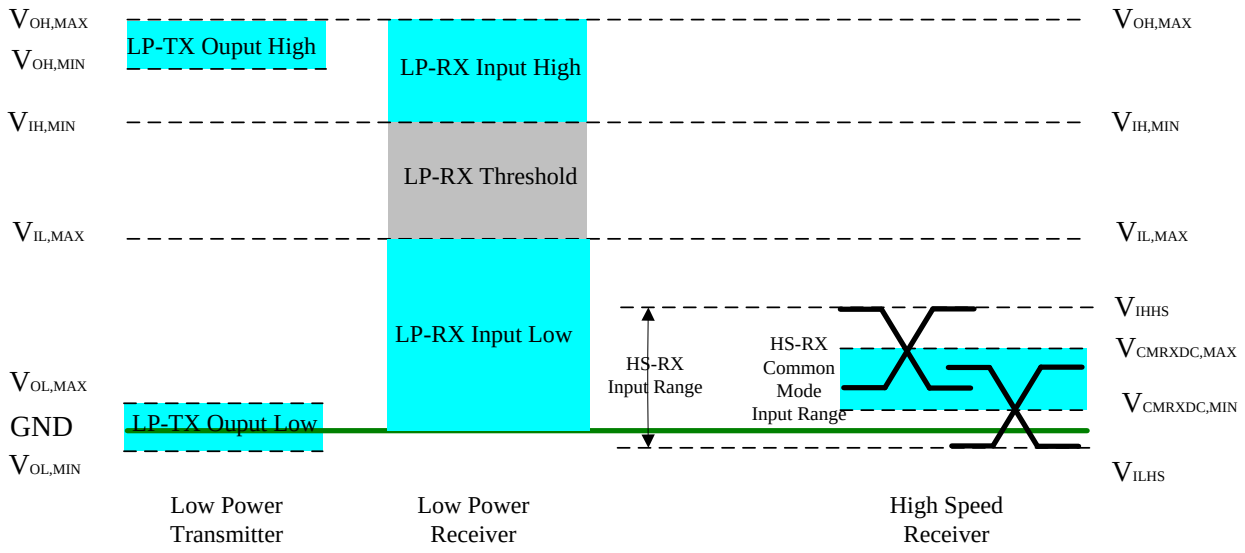
Notes:
1. Typical: VDDI=1.8V, VDD=2.8V; Ta=25 ℃

2. The Max. value is between measured point of source output and gamma setting value.

3. When evaluating the maximum and minimum of VGH, VDD=2.8V.

4. The maximum value of |VGH-VGL| can no over 30V.

7.3 DC Characteristics



VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Parameter	Symbol	Specification			Unit
		MIN	TYP	MAX	
Operation Voltage for MIPI Receiver					
Low power mode operating voltage	V_{LPH}	1.1	1.2	1.3	V
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Common-mode voltage	V_{CMRXDC}	70	-	330	mV
Differential input impedance	Z_{ID}	80	100	125	ohm
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	V_I	-50	-	1350	mV
Logic 0 input threshold	V_{IL}	0-	-	550	mV
Logic 1 input threshold	V_{IH}	880	-	1350	mV
Output low level	V_{OL}	-50	-	50	mV
Output high level	V_{OH}	1.1	1.2	1.3	V

7.4 Power Consumption

RGB Interface

Ta=25℃, Frame rate = 60Hz, Registers setting are IC default setting.

Operation Mode	Image	Current Consumption			
		Typical		Maximum	
		IDDI (uA)	IDD (uA)	IDDI (uA)	IDD (uA)
Sleep-in mode	--	5	45	10	60

MIPI Interface

Ta=25℃, Frame rate = 60Hz, Registers setting are IC default setting.

Operation Mode	Image	Current Consumption			
		Typical		Maximum	
		IDDI (uA)	IDD (uA)	IDDI (uA)	IDD (uA)
Sleep-in mode	--	5	70	10	150

Table 3 Power Consumption

Notes:
1. The Current Consumption is DC characteristics of ST7701S.
2. Typical: VDDI=1.8V, VDD=2.8V;

7.5 AC Characteristics

7.5.1 Serial Interface Characteristics (3-line serial):

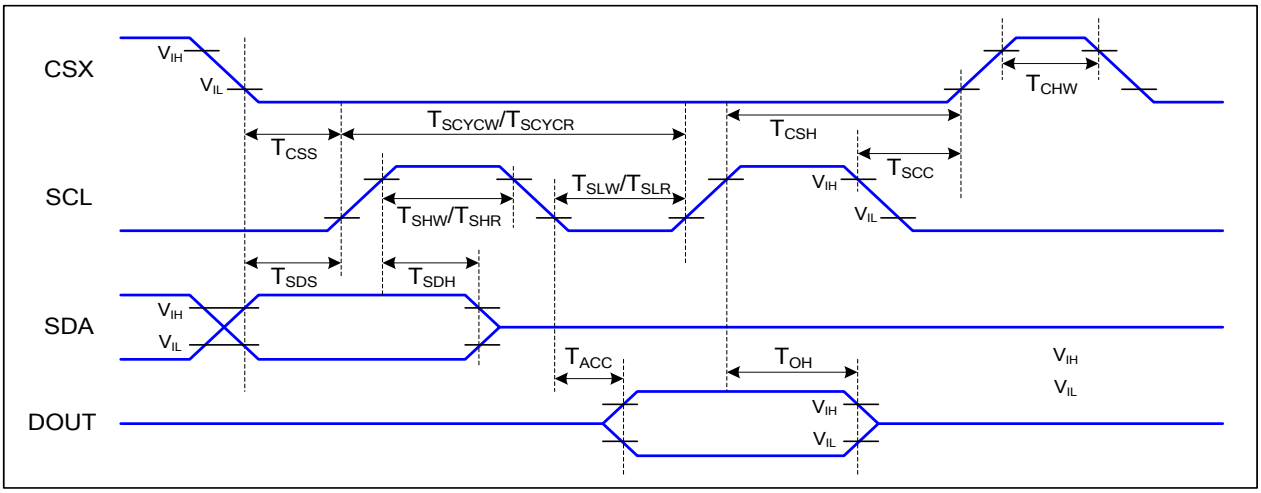


Figure 1 3-line serial Interface Timing Characteristics

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	60		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL “H” pulse width (Write)	15		ns	
	T_{SLW}	SCL “L” pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	

Table 4 3-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.5.2 Serial Interface Characteristics (4-line serial):

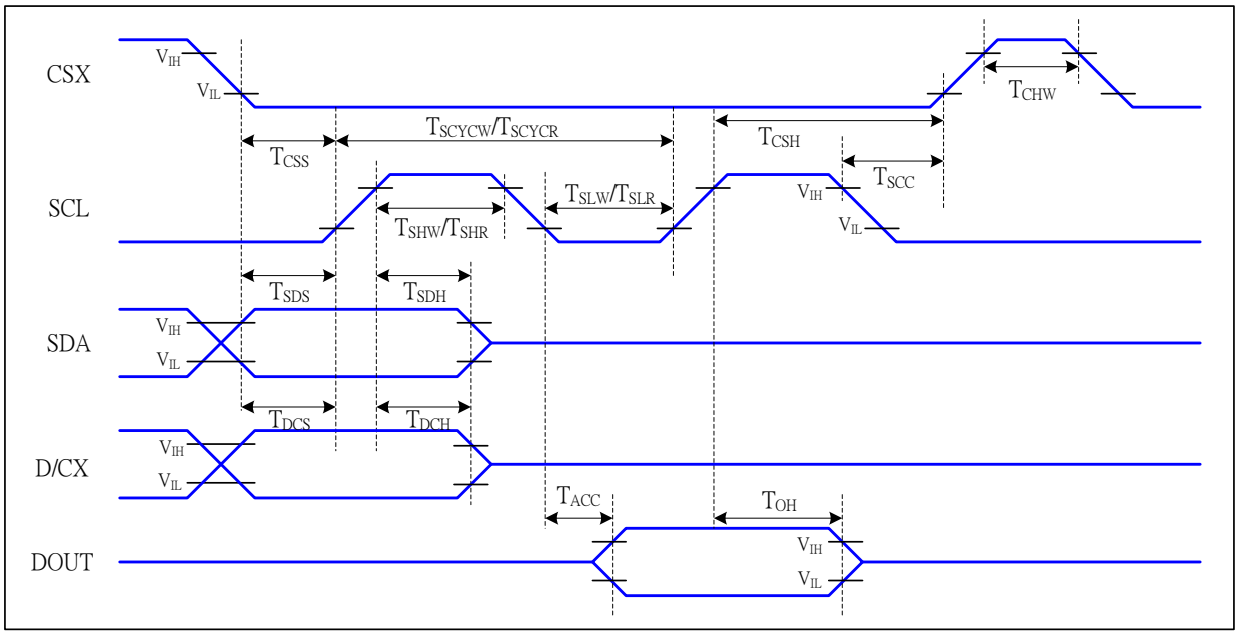


Figure 2 4-line serial Interface Timing Characteristics

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL “H” pulse width (Write)	15		ns	
	T_{SLW}	SCL “L” pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	

Table 5 4-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.5.3 RGB Interface Characteristics :

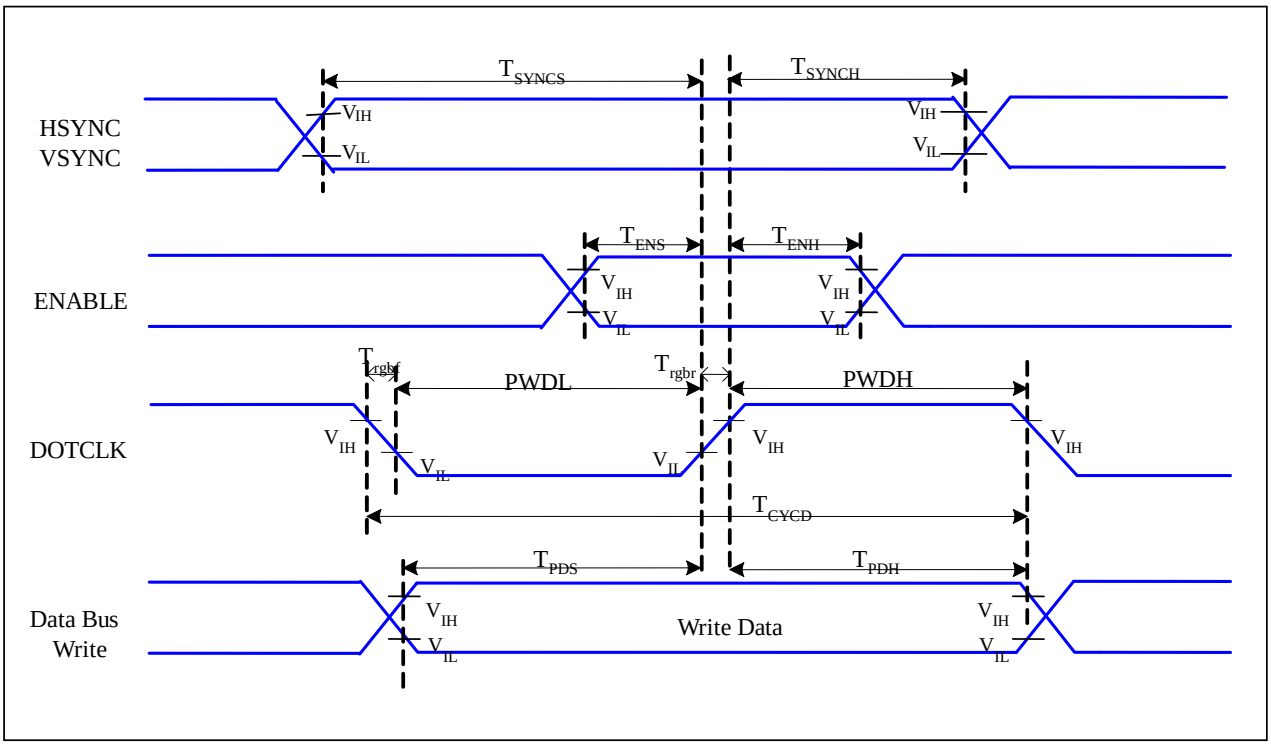


Figure 3 RGB Interface Timing Characteristics

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	5	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	5	-	ns	
	T_{ENH}	Enable Hold Time	5	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	15	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	15	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	33	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	15	ns	
DB	T_{PDS}	PD Data Setup Time	5	-	ns	
	T_{PDH}	PD Data Hold Time	5	-	ns	

Table 6 18/16 Bits RGB Interface Timing Characteristics

7.5.4 MIPI Interface Characteristics:

7.5.4.1 High Speed Mode

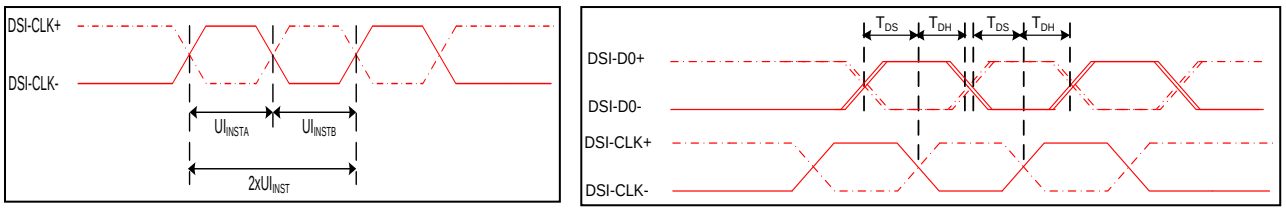


Figure 4 DSI clock channel timing

Figure 5 Rising and falling time on clock and data channel

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	4	25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	2	12.5	ns	$UI = UI_{INSTA} = UI_{INSTB}$
DSI-Dn+/-	tDS	Data to clock setup time	0.15	-	UI	
DSI-Dn+/-	tDH	Data to clock hold time	0.15	-	UI	

Table 7 Mipi Interface- High Speed Mode Timing Characteristics

7.5.4.2 Lowe Power Mode

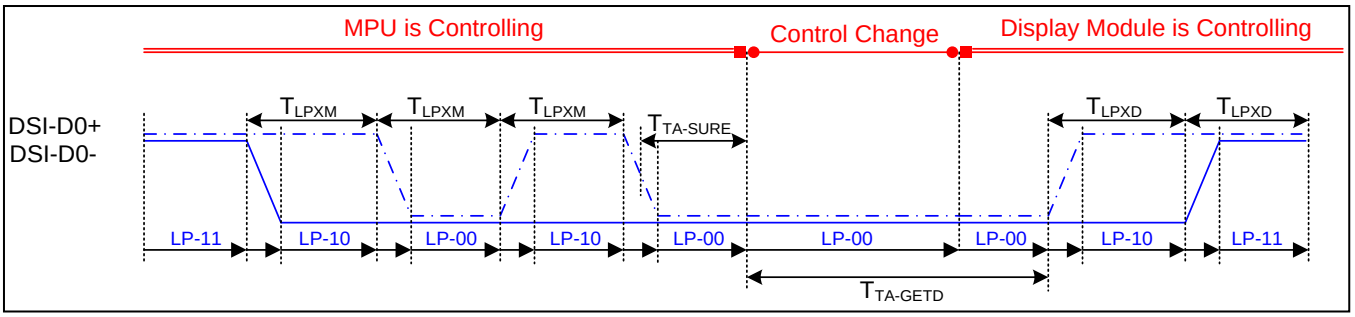


Figure 6 Bus Turnaround (BTA) from display module to MPU Timing

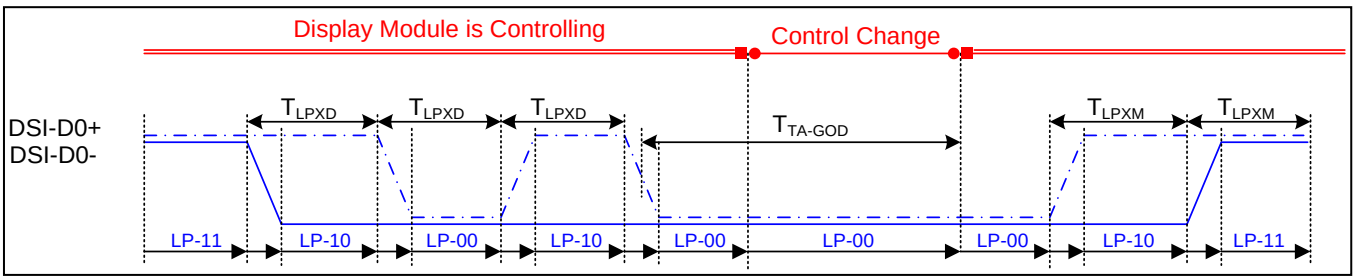


Figure 7 Bus Turnaround (BTA) from MPU to display module Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	T_{LPXD}	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5xT_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4xT_{LPXD}$		ns	Output

Table 8 Mipi Interface Low Power Mode Timing Characteristics

7.5.4.3 DSI Bursts Mode

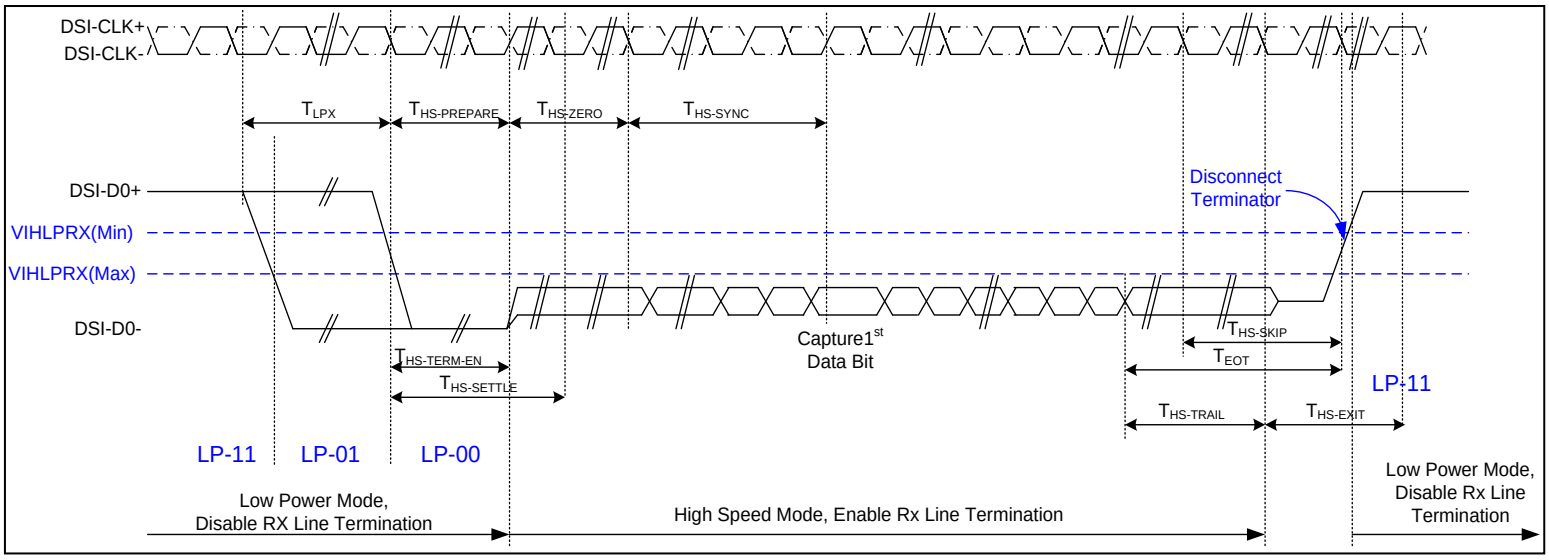


Figure 7 Data lanes-Low Power Mode to/from High Speed Mode Timing

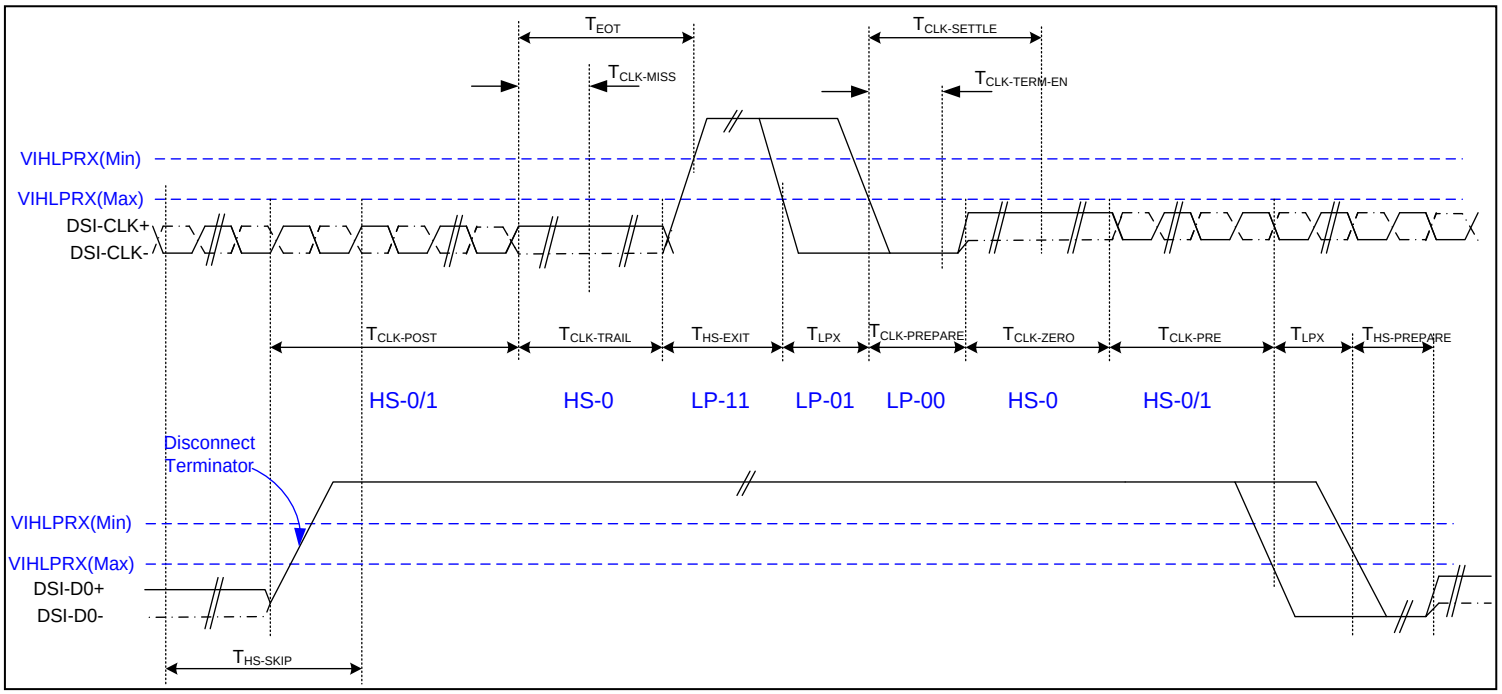


Figure 8 Clock lanes- High Speed Mode to/from Low Power Mode Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+6 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+ 10UI	-	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4 UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4 UI	-	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 2UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	--	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105n s+12 UI	ns	Input

7.5.5 Reset Timing:

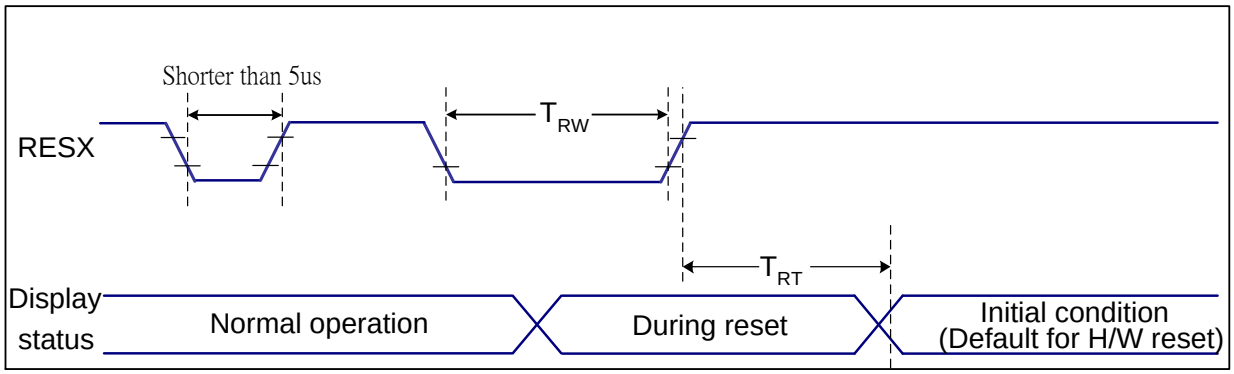


Figure 9 Reset Timing

VDDI=1.8,VDD=2.8, AGND=DGND=0V, Ta=25 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120(Note 1, 6, 7)	ms

Table 9 Reset Timing

Notes:

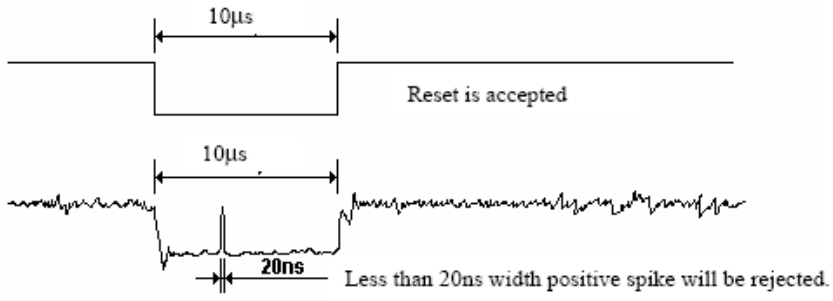
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8 FUNCTION DESCRIPTION

8.1 System Interface

ST7701S supports RGB serial interfaces , and MIPI serial interfaces. Selection of these interfaces are set by IM[3:0] pins as shown below.

IM3	IM2	IM1	IM0	Interface	Data pins
0	0	0	1	RGB+8b_SPI(fall)	D[0~23]
	0	1	0	RGB+9b_SPI(fall)	D[0~23]
	0	1	1	RGB+16b_SPI(rise)	D[0~23]
	1	0	1	MIPI	HSSI_D1_P/N,HSSI_D0_P/N
	1	1	0	MIPI+16b_SPI(rise)	HSSI_D1_P/N,HSSI_D0_P/N
1	0	0	1	RGB+8b_SPI(rise)	D[0~23]
	0	1	0	RGB+9b_SPI(rise)	D[0~23]
	0	1	1	RGB+16b_SPI(fall)	D[0~23]
	1	0	1	MIPI	HSSI_D1_P/N,HSSI_D0_P/N
	1	1	0	MIPI+16b_SPI(fall)	HSSI_D1_P/N,HSSI_D0_P/N

Table 10 Interface Type Selection

8.2 Serial Interface

The serial interface is either 3-lines/9-bits,16-bits or 4-lines/8-bits bi-directional interface for communication between the micro controller and the LCD driver. The 3-lines serial interface use: CSX (chip enable), SCL (serial clock) and SDA (serial data input/output), and the 4-lines serial interface use: CSX (chip enable), D/CX (data/ command flag), SCL (serial clock) and SDA (serial data input/output). Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

Pin description

3-line serial interface (9 bits)

Pin Name	Description
CSX	Chip selection signal
SCL	Serial input CLK
SDA	Serial input data
SDO	Serial output data

4-line serial interface (8 bits)

Pin Name	Description
CSX	Chip selection signal
DCX	Data is regarded as a command when SCL is low Data is regarded as a parameter or data when SCL is high
SCL	Clock signal
SDA	Serial input data
SDO	Serial output data

8.2.1 Serial Interface (SPI)

8.2.1.1 Command write mode

The write mode of the interface means the micro controller writes commands and data to the LCD driver. 3-lines serial data packet contains a control bit D/CX and a transmission byte. In 4-lines serial interface, data packet contains just transmission byte and control bit D/CX is transferred by the D/CX pin. If D/CX is “low”, the transmission byte is interpreted as a command byte. If D/CX is “high”, the transmission byte is command register as parameter.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

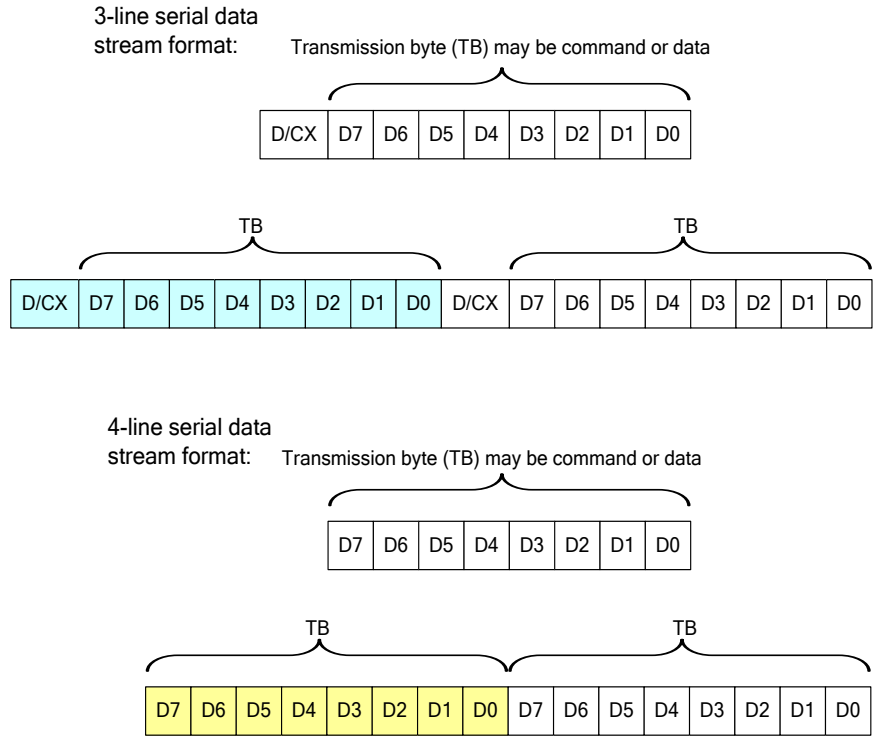


Figure 10 Serial interface data stream format

When CSX is “high”, SCL clock is ignored. During the high period of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low. SDA is sampled at the rising edge of SCL. D/CX indicates whether the byte is command (D/CX=’0’) or parameter data (D/CX=’1’). D/CX is sampled when first rising edge of SCL (3-line serial interface) or 8th rising edge of SCL (4-line serial interface). If CSX stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-line serial interface) or D7 (4-line serial interface) of the next byte at the next rising edge of SCL..

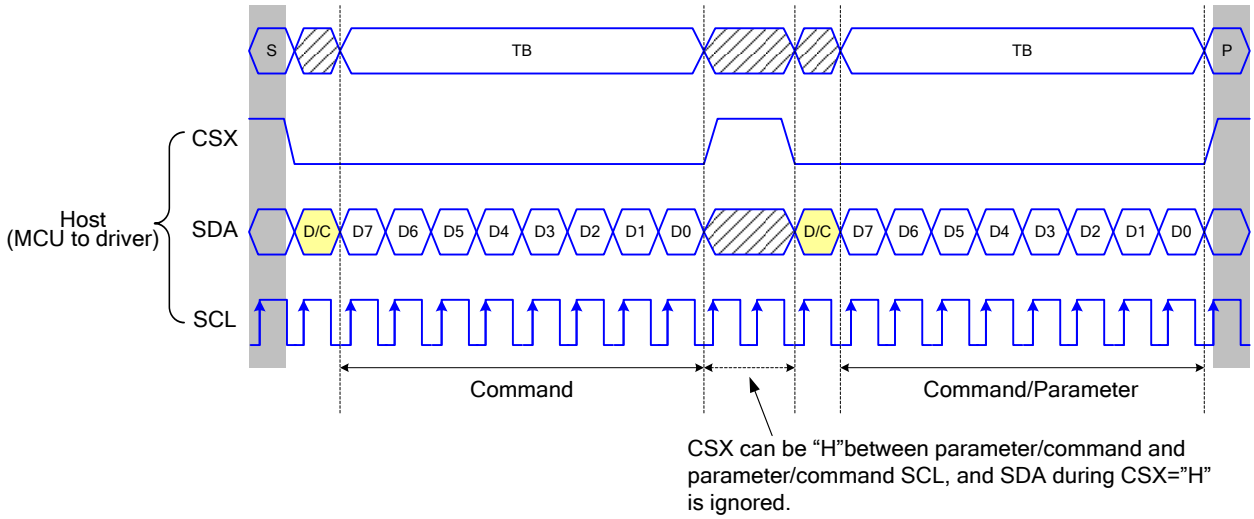


Figure 11 3-line serial interface write protocol (write to register with control bit in transmission)

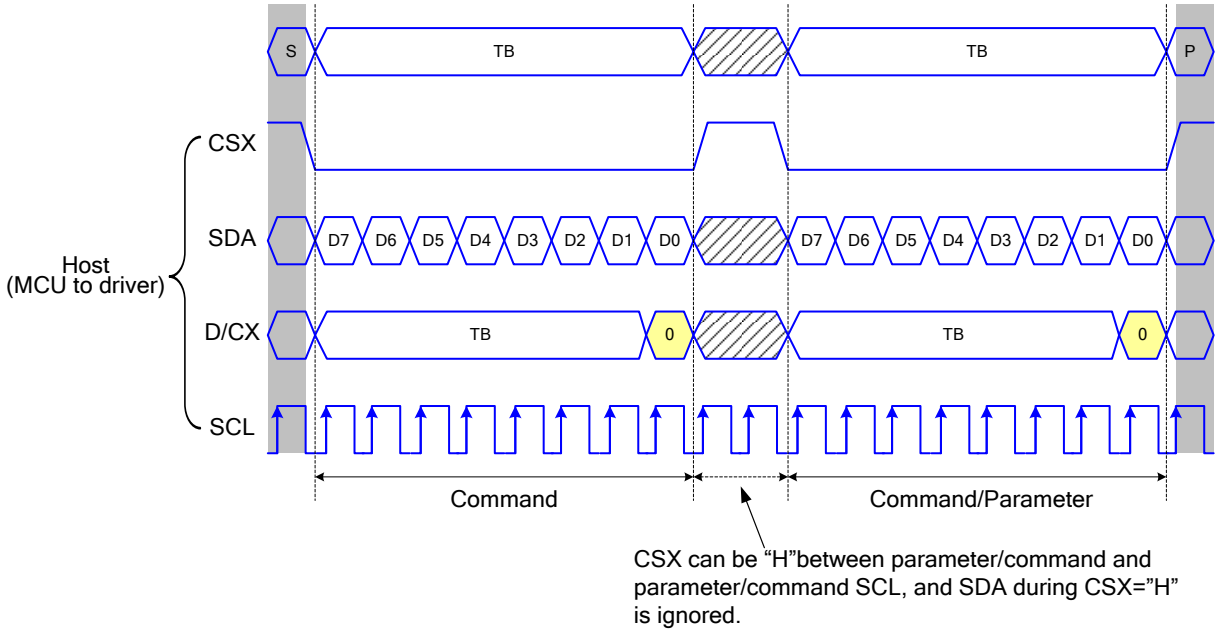


Figure 12 4-line serial interface write protocol (write to register with control bit in transmission)

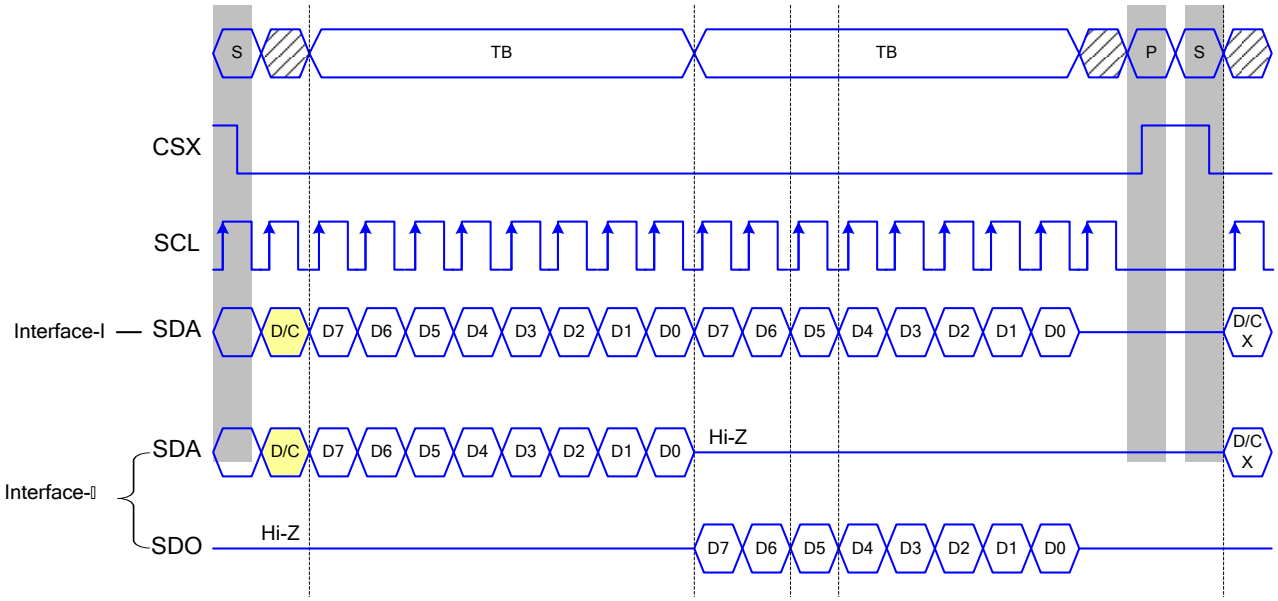
8.2.2 Read function

The read mode of the interface means that the micro controller reads register value from the driver. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

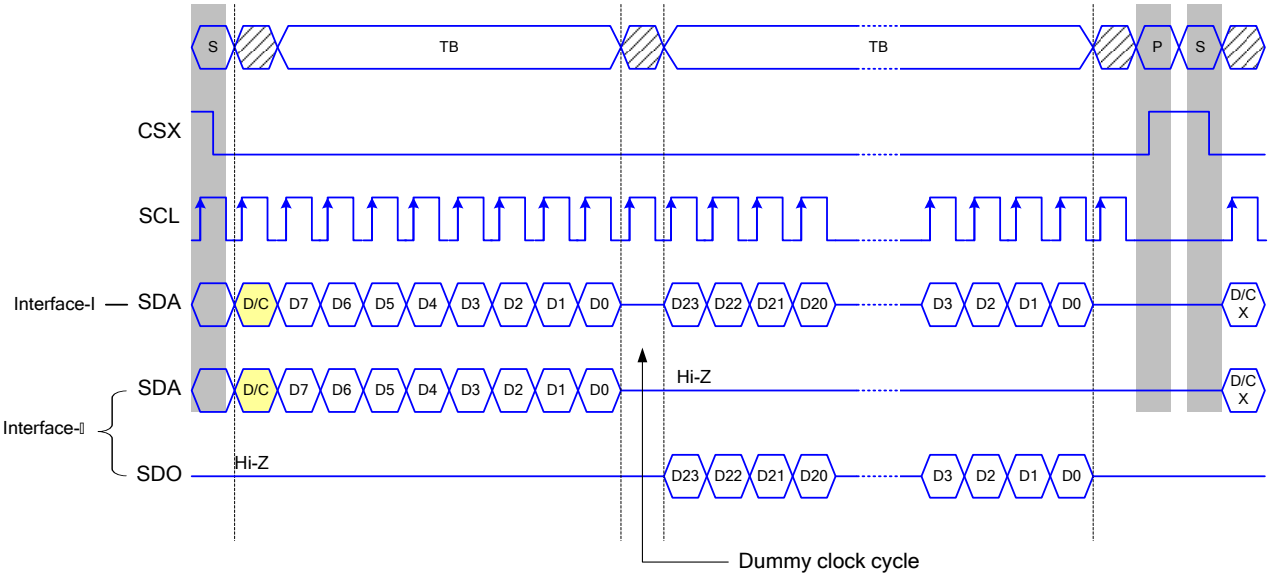
After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

3-line serial interface protocol

3-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



3-line serial protocol (for RDDID command: 24-bit read)



3-line Serial Protocol (for RDDST command: 32-bit read)

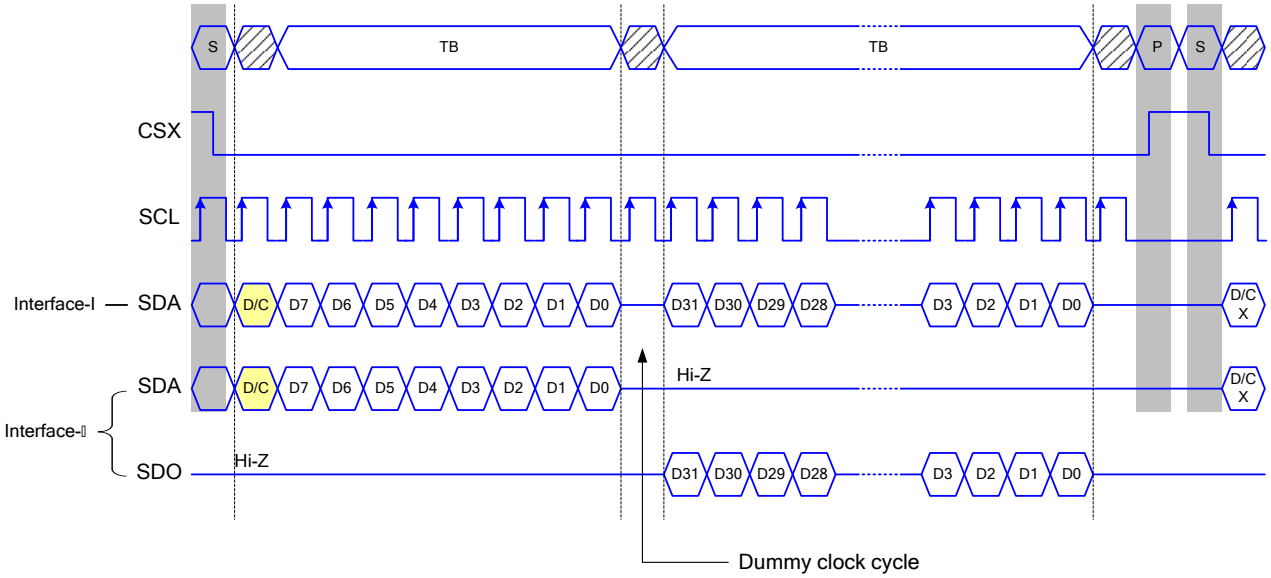
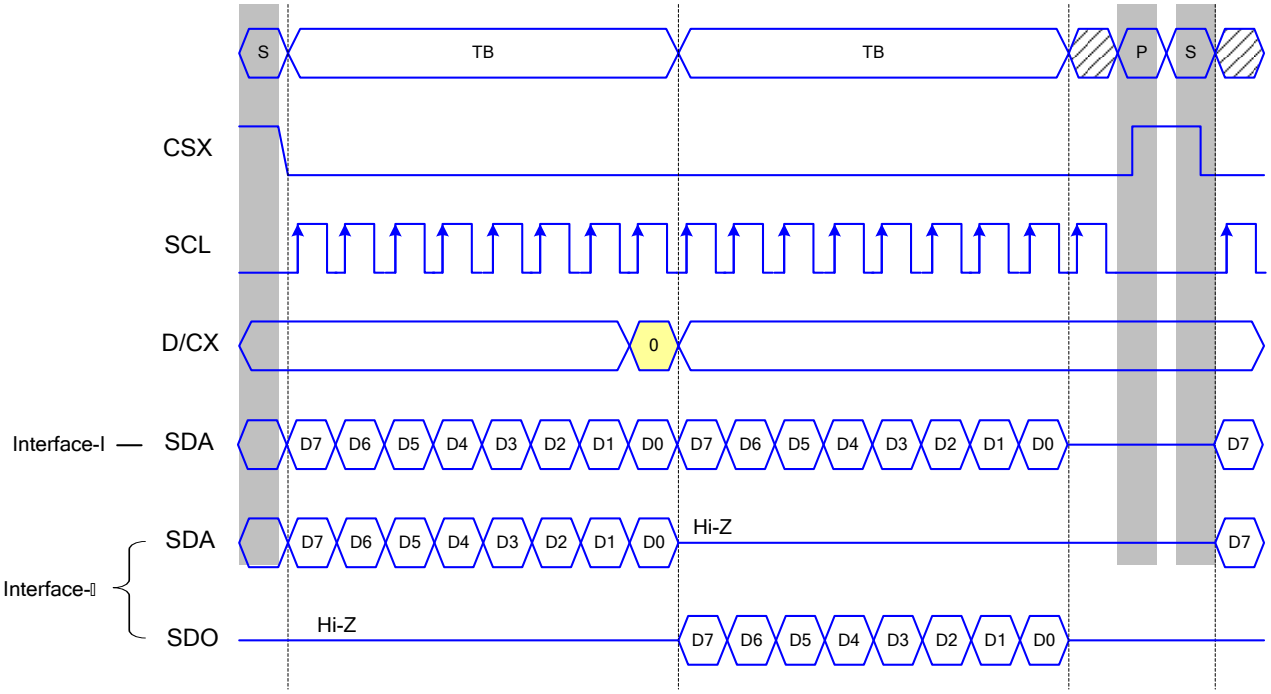


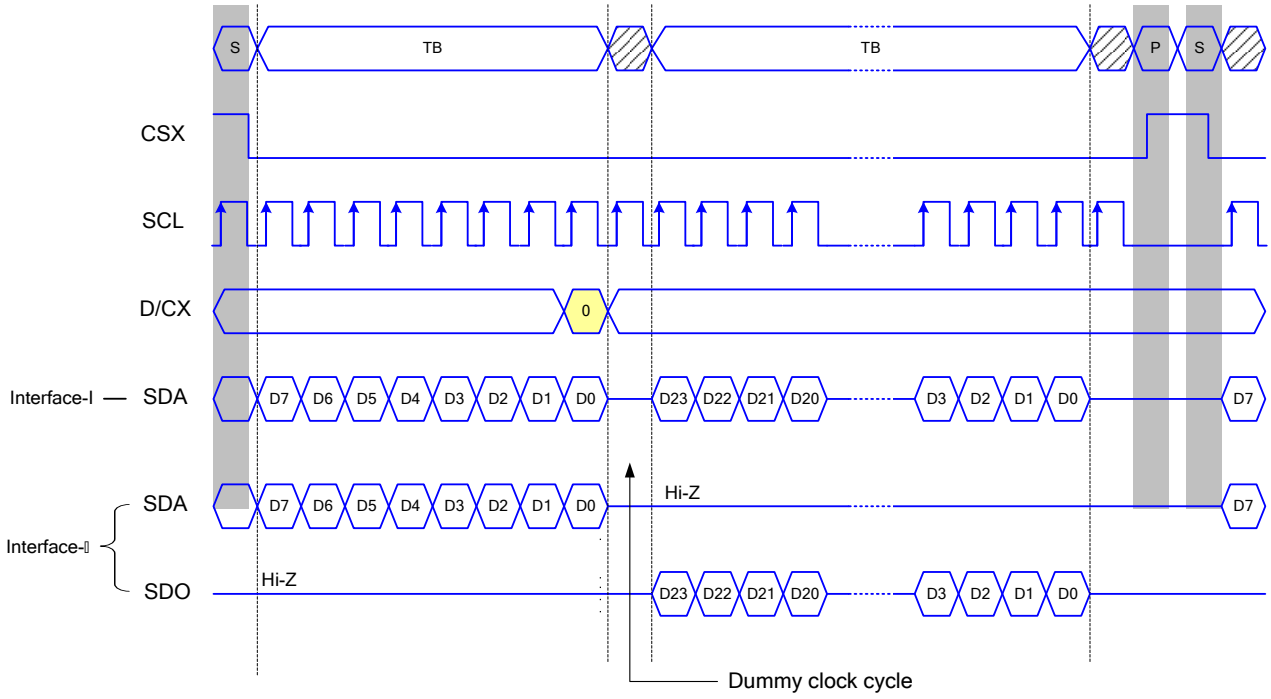
Figure 13 3-line serial interface read protocol

4-line serial protocol

4-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



4-line serial protocol (for RDDID command: 24-bit read)



4-line Serial Protocol (for RDDST command: 32-bit read)

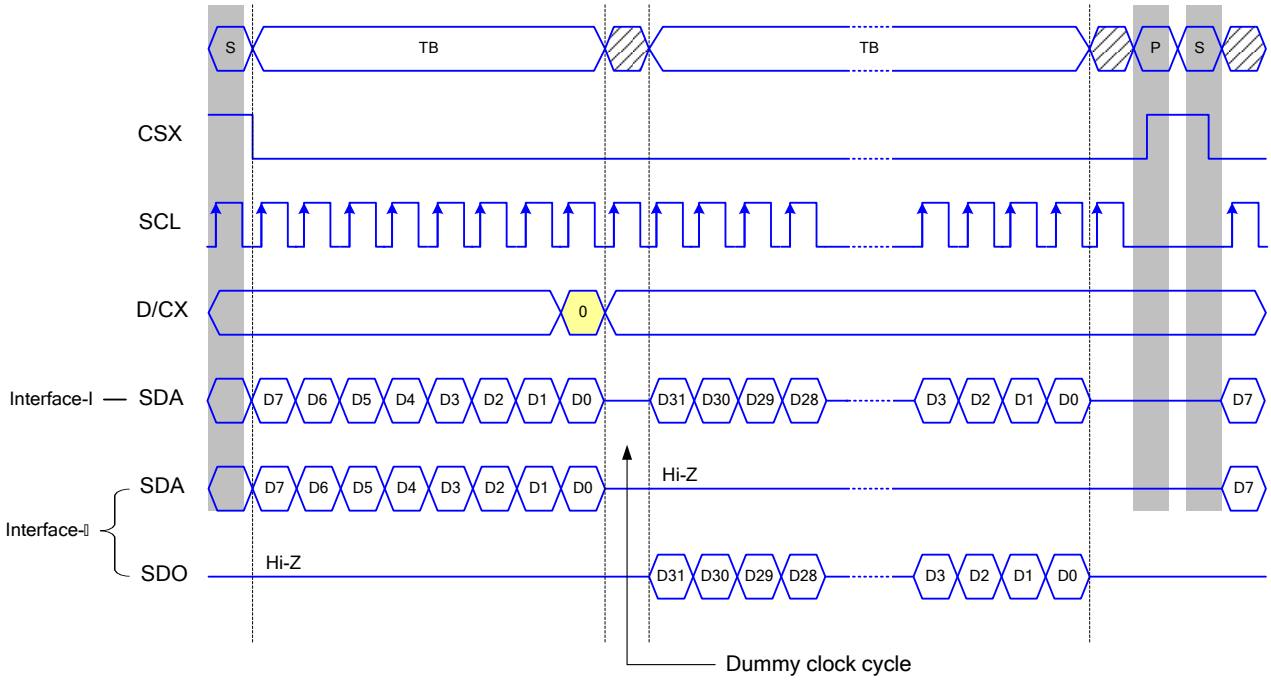


Figure 14 4-line serial interface read protocol

8.3 16 bit Serial Interface

8.3.1 Write Mode

The write mode of the interface means the micro controller writes commands and data to the ST7701S. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

When CSX is high, SCL clock is ignored. During the high time of CSX the serial interface is initialized. At the falling CSX edge, SCL can be high or low. SDI/SDO are sampled at the rising edge of SCL. R/W indicates, whether the byte is read command (R/W = '1') or write command (R/W = '0'). It is sampled when first rising SCL edge. If CSX stays low after the last bit of command/data byte, the serial interface expects the R/W bit of the next byte at the next rising edge of SCL.

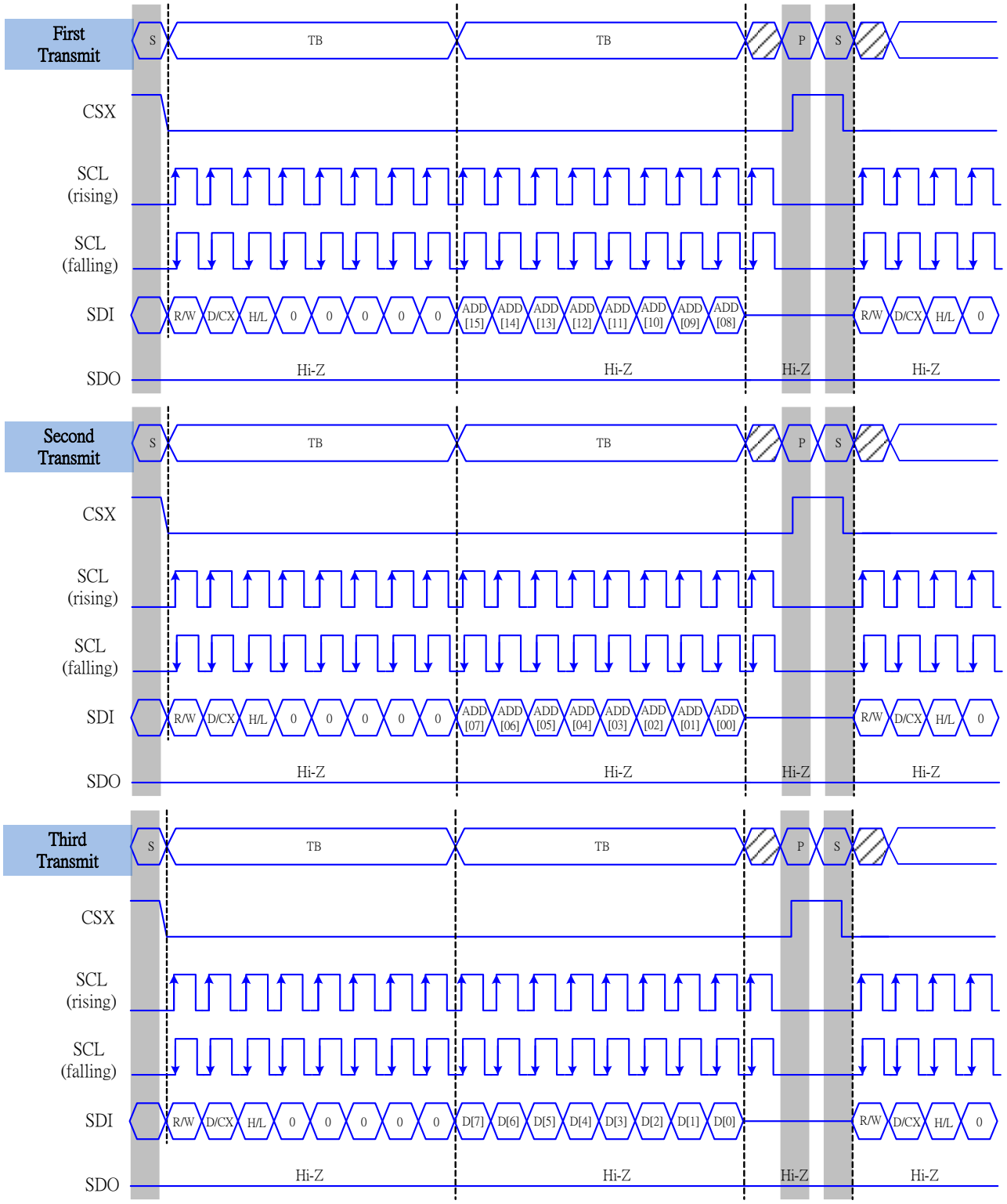


Figure 15 serial 16 bit interface write mode

8.3.2 Read Mode

The read mode of the interface means that the micro controller reads register value from the ST7701S. To do so the micro controller first has to send a command and then the following byte is transmitted in the opposite direction. After that CSX is required to go high before a new command is send. The ST7701S samples the SDI (input data) at the rising edges, but shifts SDO (output data) at the falling SCL edges. Thus the micro controller is supported to read data at the rising SCL edges. After the read status command has been sent, the SDI line must be set to tri-state no later than at the falling SCL edge of the last bit. It doesn't need any dummy clock when execute the command data read.

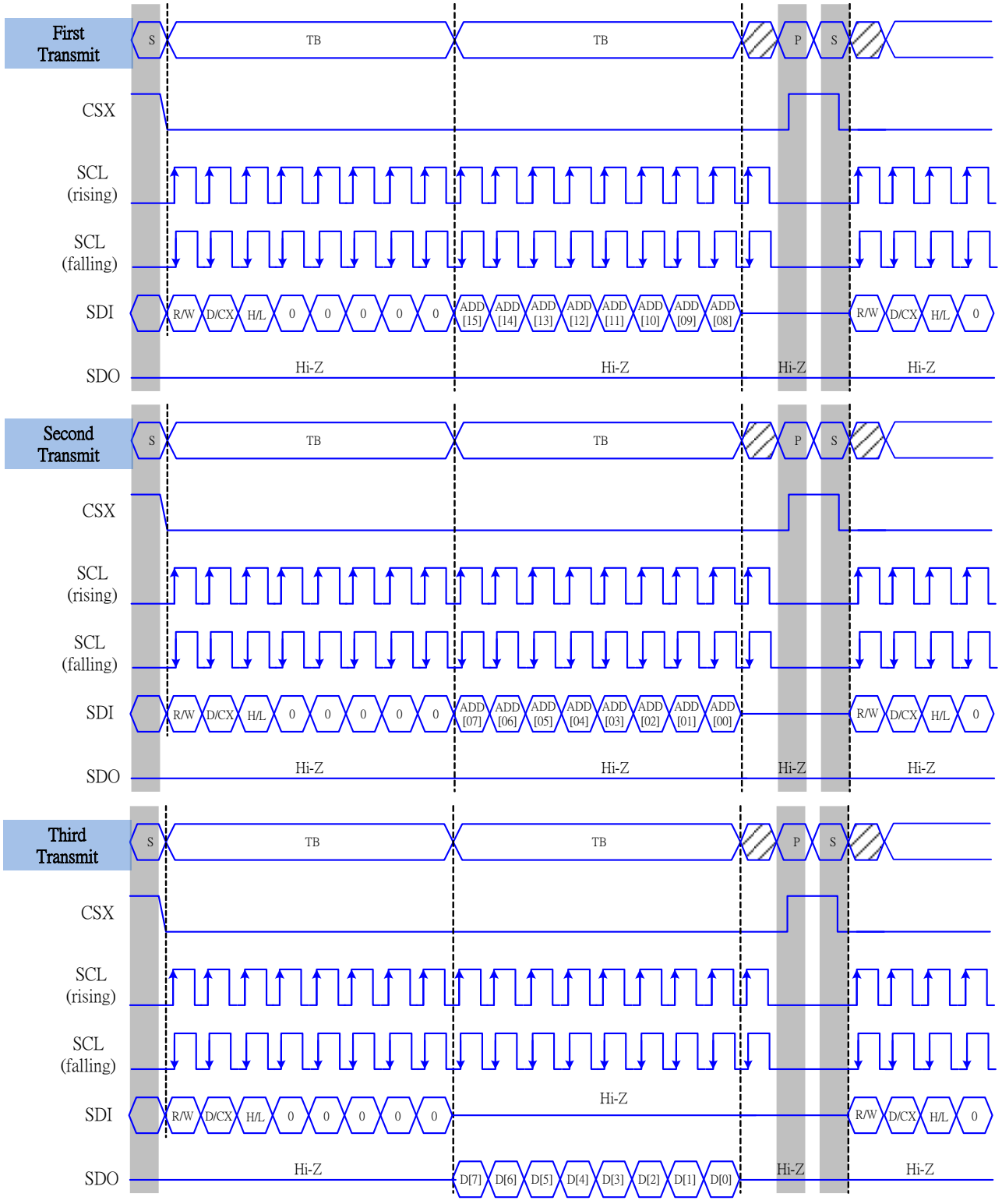


Figure 16 serial 16 bit interface read mode

8.4 Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been HIGH state.

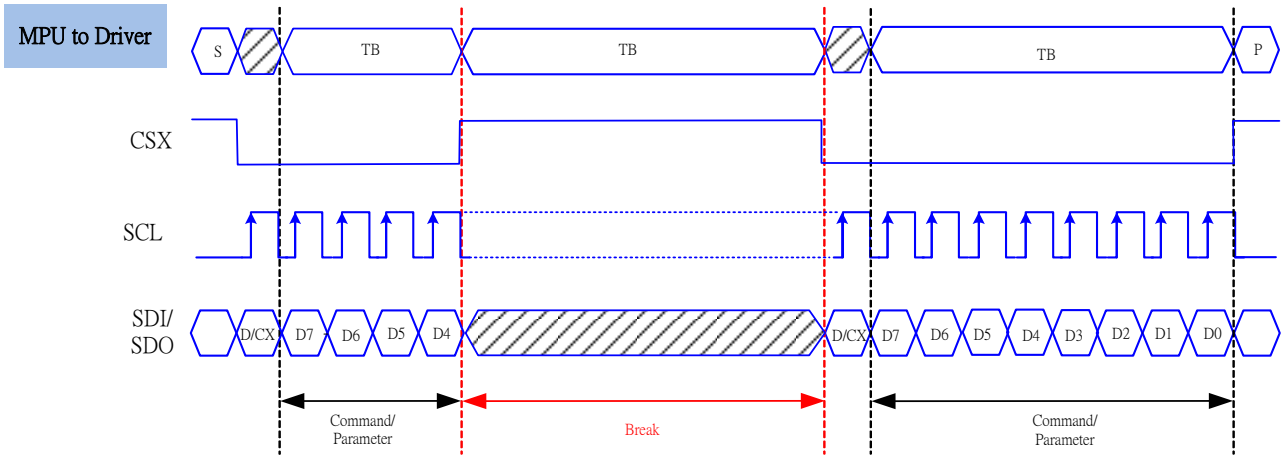


Figure 17 Data Transfer Break and Recovery.

If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated.

If 1, 2 or more parameter commands are being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

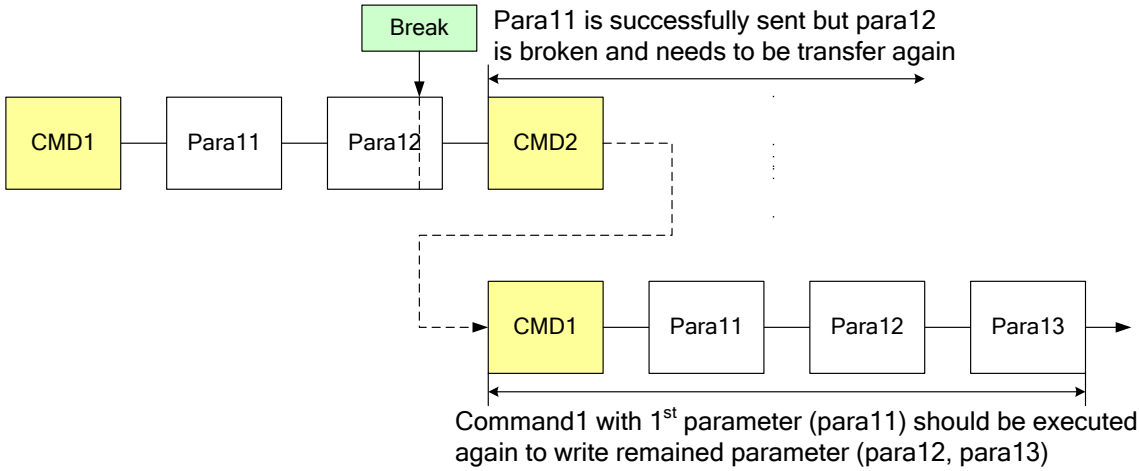


Figure 18 Write interrupts recovery

If a 2 or more parameter commands are being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

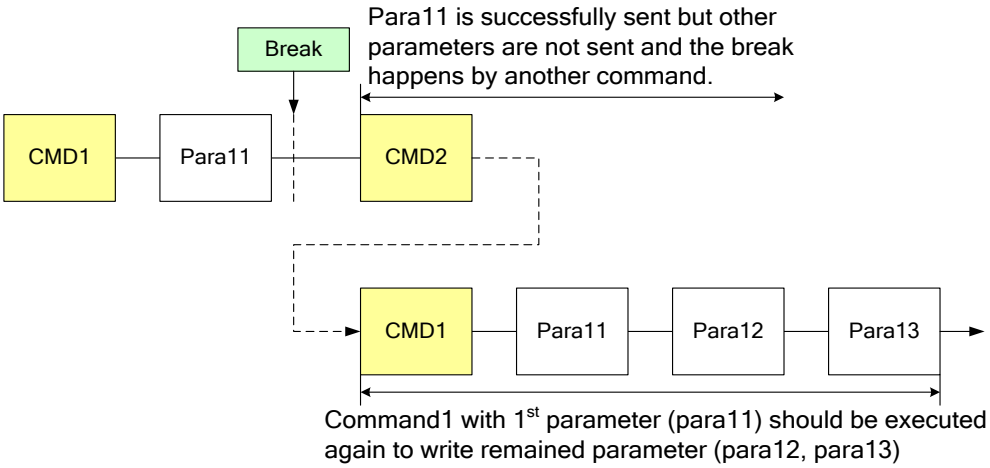


Figure 19 Write interrupts recovery

8.5 Data Transfer Pause

Transferring a Command, Frame Memory Data, or Multiple Parameter Data might invoke a pause in the data transmission. If the Chip Select pin (CSX) is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then the ST7701S will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select pin is released after a whole byte of a command has been completely transmitted, then the display module will receive either the command's parameters or a new command when the Chip Select Line is enabled again, as shown below.

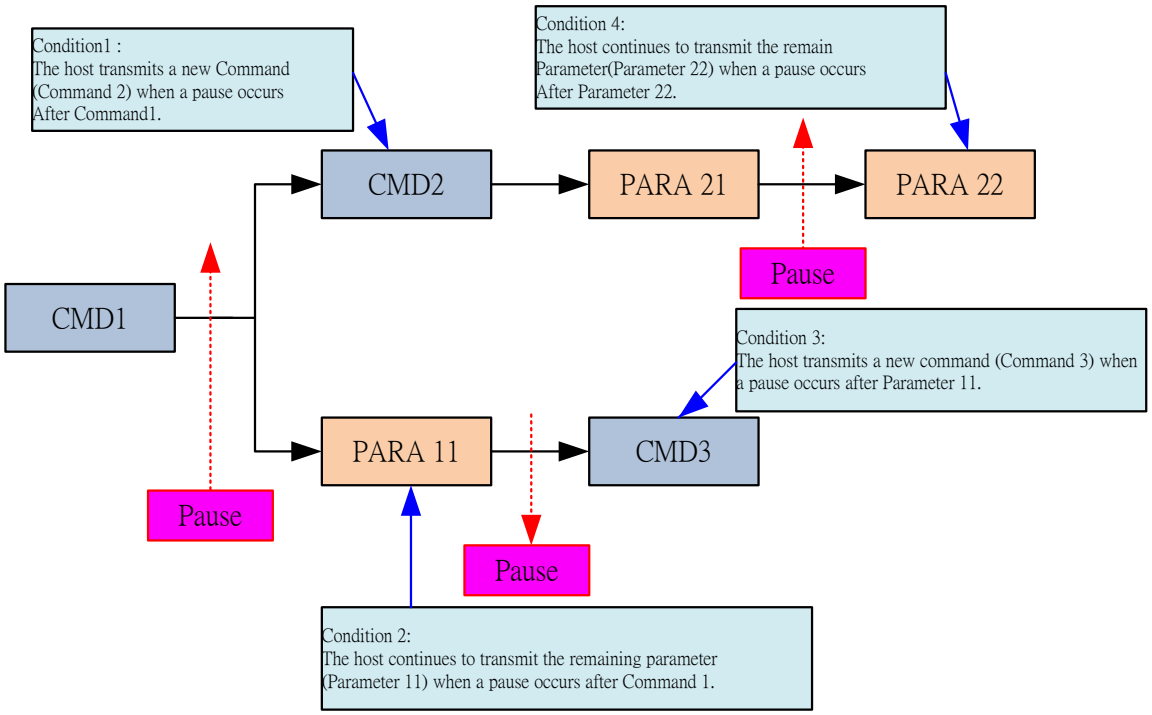


Figure 20 Data Transfer Pause

8.5.1 SPI interface pause

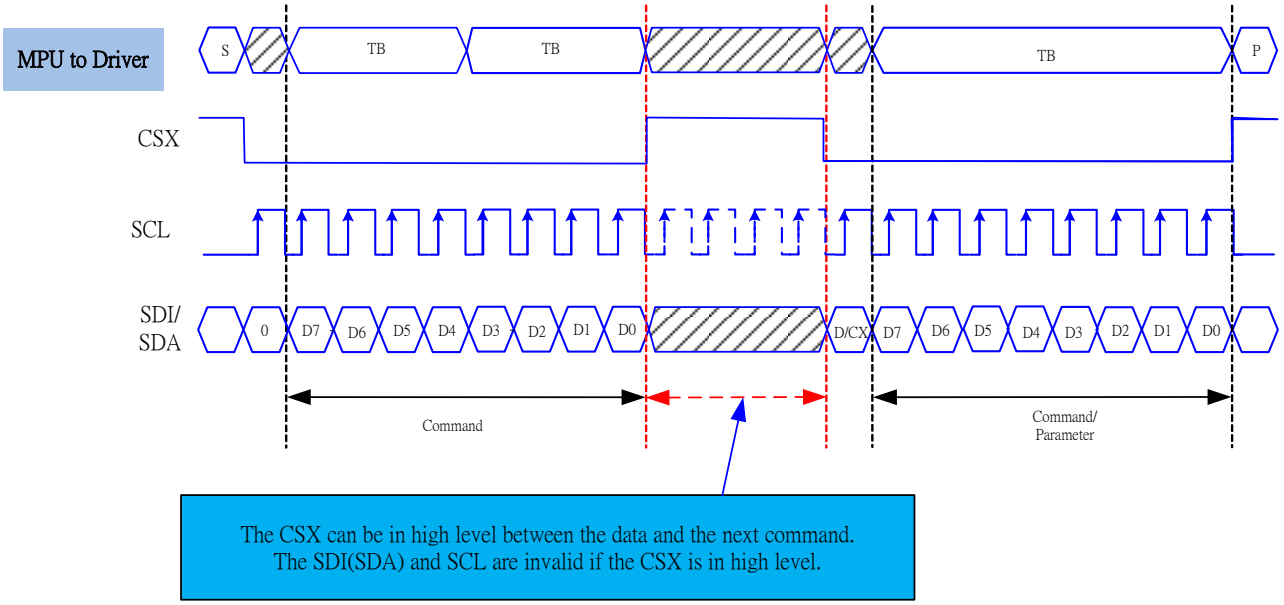


Figure 21 Serial Data Transfer Pause

This applies to the following 4 conditions:

1) Command-Pause-Command

2) Command-Pause-Parameter

3) Parameter-Pause-Command

4) Parameter-Pause-Parameter

8.6 RGB Interface

The ST7701S support RGB interface Mode 1 and Mode 2. The interface signals as shown in table 6.3.1.

The Mode 1 and Mode 2 function is select by setting in the Command 2, please reference application note.

In RGB Mode 1, writing data to line buffer is done by PCLK and Video Data Bus (D[23:0]), when DE is high state. The external clocks (PCLK, VS and HS) are used for internal displaying clock. So, controller must always transfer PCLK, VS and HS signal to ST7701S.

In RGB Mode 2, back porch of Vsync is defined by VBP[5:0] of RGBPRCTR command. And back porch of Hsync is defined by HBP[5:0] of RGBPRCTR command. Front porch of Vsync is defined by VFP[5:0] of RGBPRCTR command. And front porch of Hsync is defined by HFP[5:0] of RGBPRCTR command.

RGB I/F Mode	PCLK	DE	VS	HS	DB[23:0]	Register for Blanking Porch setting
RGB Mode 1	Used	Used	Used	Used	Used	Not Used
RGB Mode 2	Used	Not Used	Used	Used	Used	Used

Symbol	Name	Description
PCLK	Pixel clock	Pixel clock for capturing pixels at display interface
HS	Horizontal sync	Horizontal synchronization timing signal
VS	Vertical sync	Vertical synchronization timing signal
DE	Data enable	Data enable signal (assertion indicates valid pixels)
DB[23:0]	Pixel data	Pixel data in 16-bit,18-bit and 24-bit format

Table 11 The interface signals of RGB interface

8.6.1 RGB Color Format

ST7701S supports two kinds of RGB interface, DE mode (mode 1) and HV mode (mode 2), and 16bit/18bit and 24 bit data format. When DE mode is selected and the VSYNC, HSYNC, DOTCLK, DE, D[23:0] pins can be used; when HV mode is selected and the VSYNC, HSYNC, DOTCLK, D[23:0] pins can be used. When using RGB interface, only serial interface can be selected.

Pad name	24 bits configuration VIPF[3:0]=0111	18 bits configuration VIPF[3:0]=0110		16 bits configuration VIPF[3:0]=0101
		MDT=0	MDT=1	
DB[23]	R7	Not used	Not used	Not used
DB[22]	R6	Not used	Not used	Not used
DB[21]	R5	R5	Not used	Not used
DB[20]	R4	R4	Not used	R4
DB[19]	R3	R3	Not used	R3
DB[18]	R2	R2	Not used	R2
DB[17]	R1	R1	R5	R1
DB[16]	R0	R0	R4	R0
DB[15]	G7	Not used	R3	Not used
DB[14]	G6	Not used	R2	Not used
DB[13]	G5	G5	R1	G5
DB[12]	G4	G4	R0	G4
DB[11]	G3	G3	G5	G3
DB[10]	G2	G2	G4	G2
DB[09]	G1	G1	G3	G1
DB[08]	G0	G0	G2	G0
DB[07]	B7	Not used	G1	Not used
DB[06]	B6	Not used	G0	Not used
DB[05]	B5	B5	B5	Not used
DB[04]	B4	B4	B4	B4
DB[03]	B3	B3	B3	B3
DB[02]	B2	B2	B2	B2
DB[01]	B1	B1	B1	B1
DB[00]	B0	B0	B0	B0

Table 12 The interface color mapping of RGB interface

8.6.2 RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.

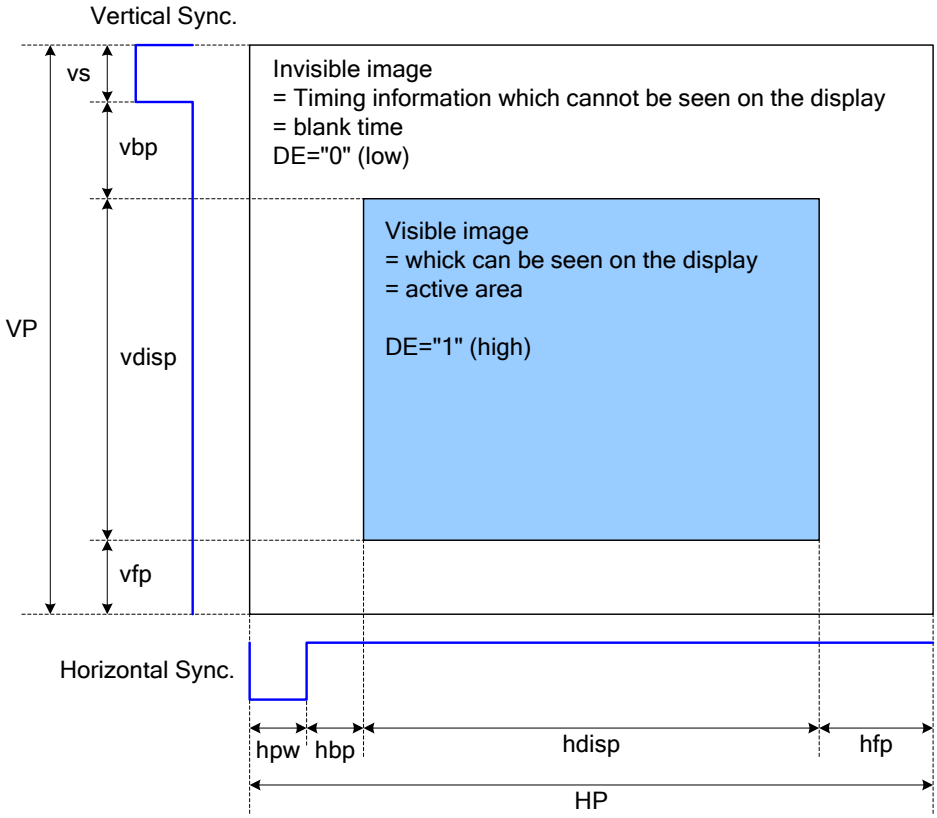


Figure 22 Access Area by RGB Interface

Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal Sync. Width	hpw	1	-	255	Clock
Horizontal Sync. Back Porch	hbp	1	--	255	Clock
Horizontal Sync. Front Porch	hfp	1	--	-	Clock
Vertical Sync. Width	vs	1	--	254	Line
Vertical Sync. Back Porch	vbp	1	--	254	Line
Vertical Sync. Front Porch	vfp	2	--	--	Line

Note:

1. Typical value are related to the setting frame rate is 60Hz..

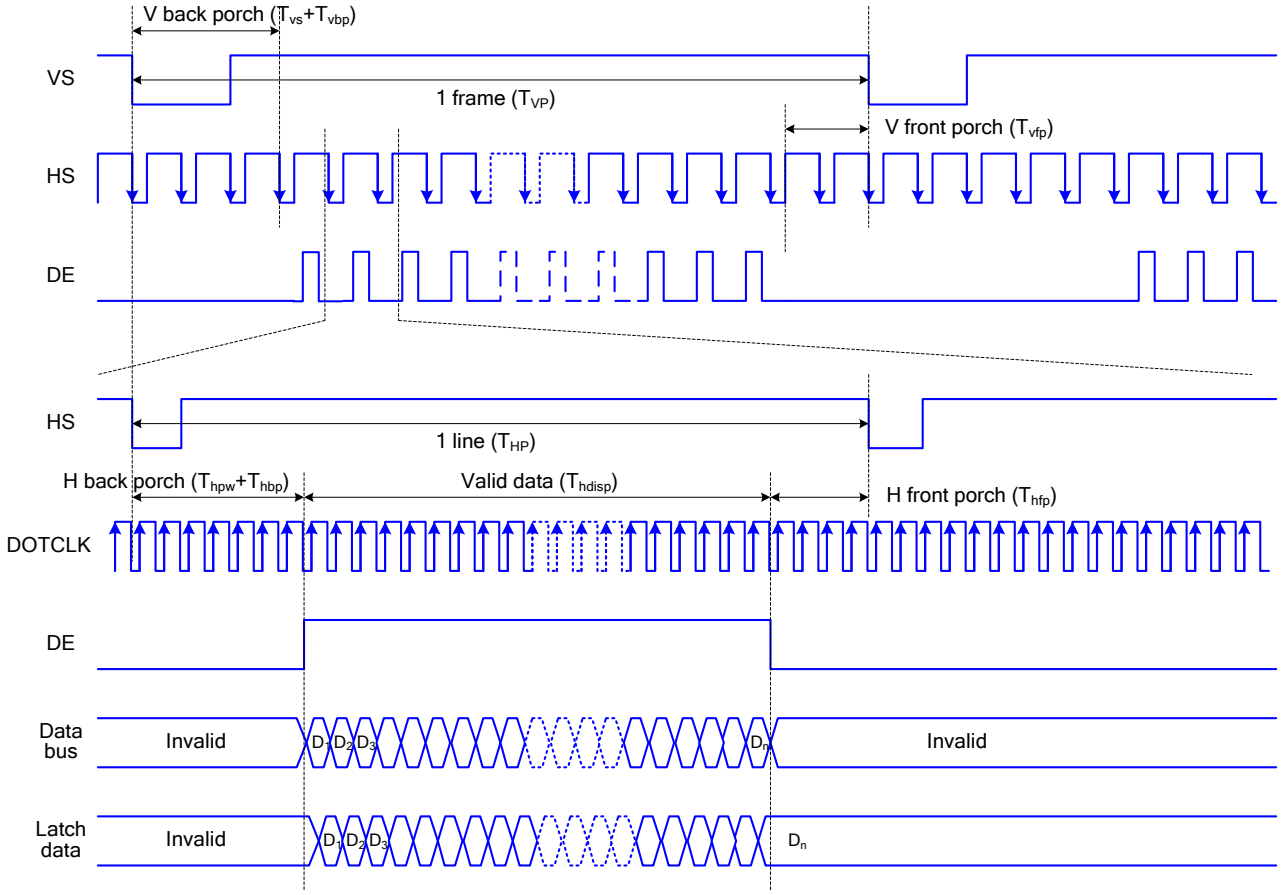
8.6.3 RGB Interface Mode Selection

ST7701S supports two kinds of RGB interface, DE mode and HV mode. The table shown below uses command C3h to select RGB interface mode.

DE/Sync	RGB Mode
0	DE mode
1	HV mode

8.6.4 RGB Interface Timing

The timing chart of RGB interface DE mode is shown as follows.



Note: The setting of front porch and back porch in host must match that in IC as this mode.

Figure 23 Timing Chart of Signals in RGB Interface DE Mode

The timing chart of RGB interface HV mode is shown as follows.

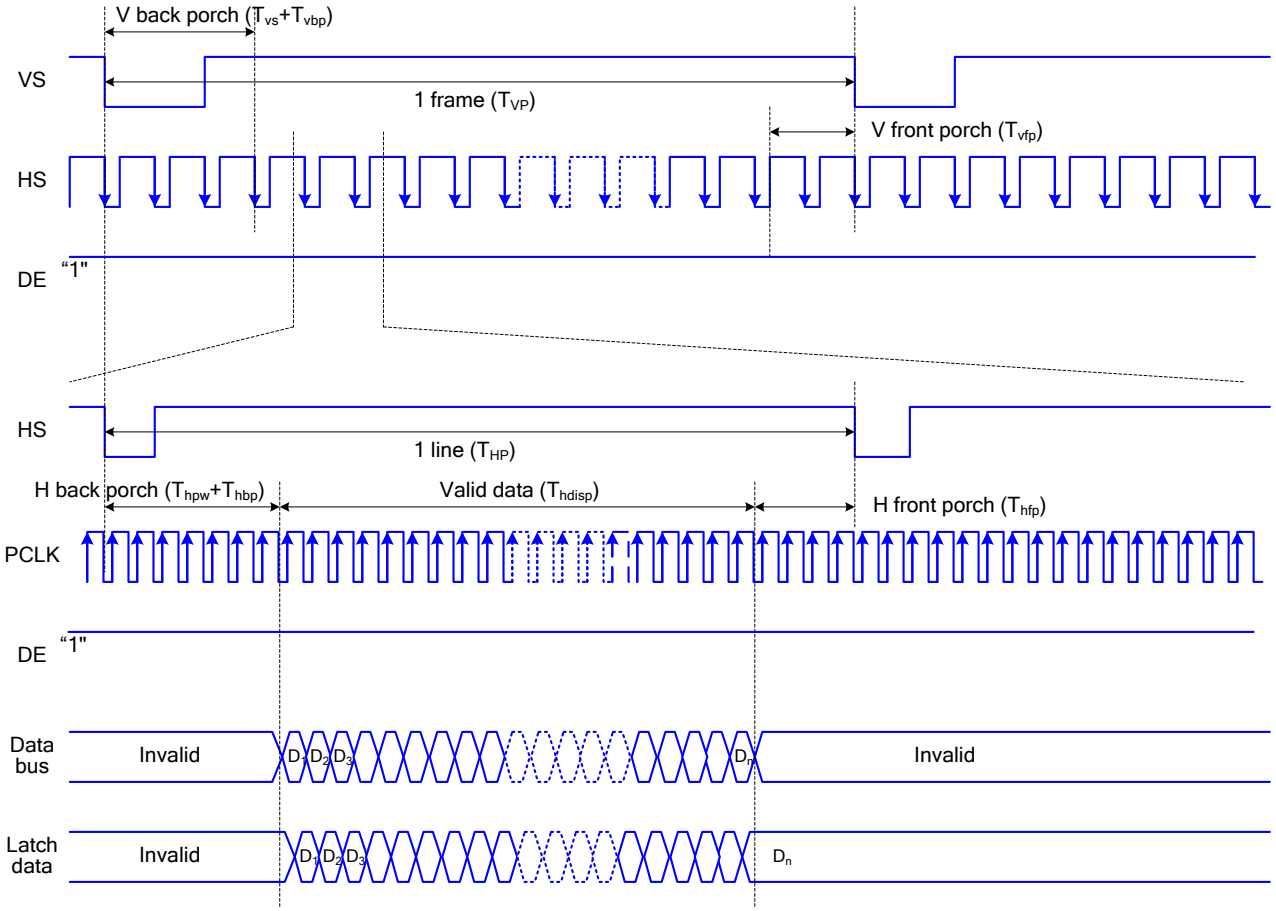


Figure 24 Timing chart of RGB interface HV mod

8.7 MIPI-DSI interface

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

Typically, a peripheral is capable of Command Mode operation or Video Mode operation. Some Video Mode display modules also include a simplified form of Command Mode operation in which the display module may refresh its screen from a reduced-size, or partial, frame buffer, and the interface (DSI) to the host processor may be shut down to reduce power consumption.

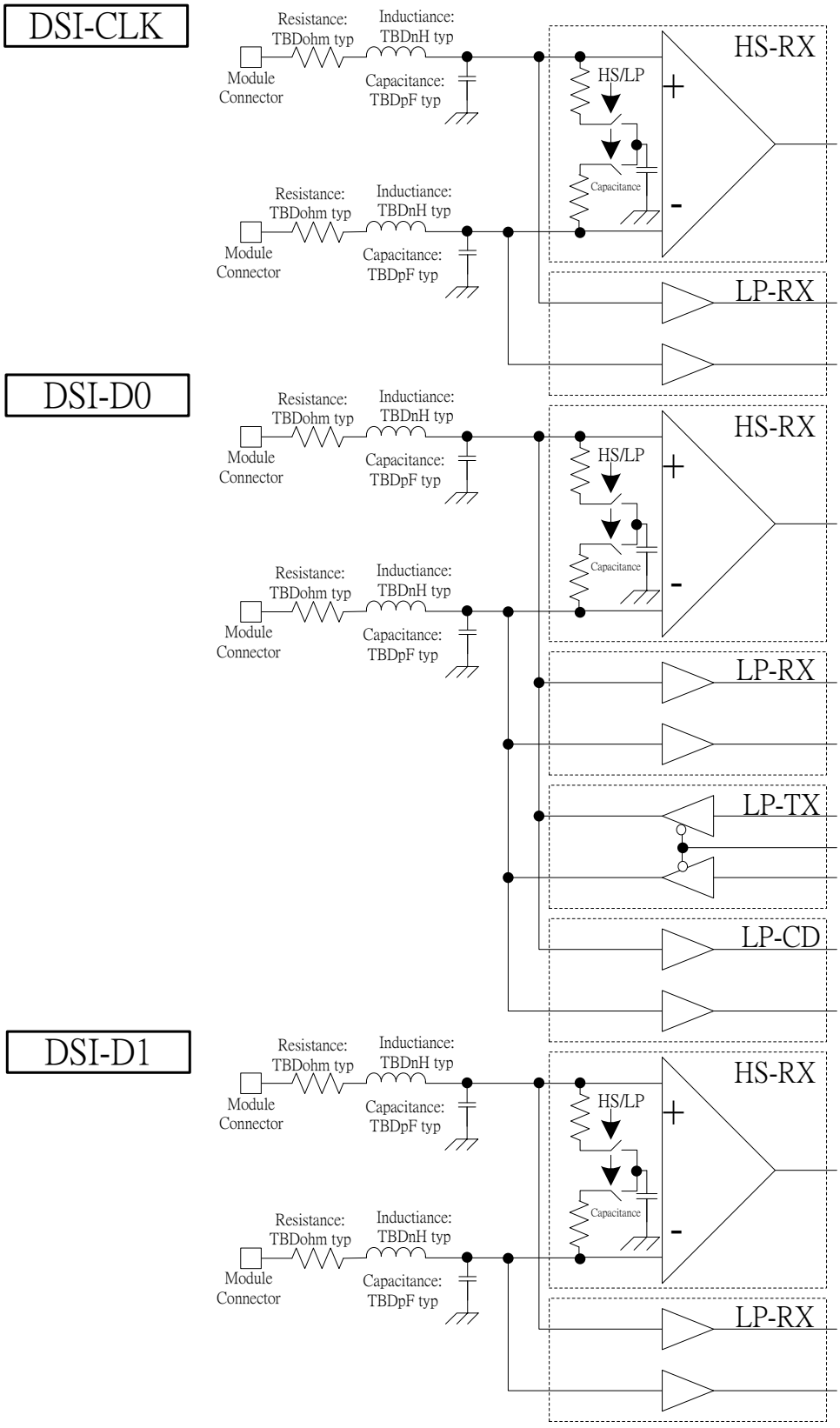
Command Mode refers to operation in which transactions primarily take the form of sending commands to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers. The host processor indirectly controls activity at the peripheral by sending commands, parameters to the display controller. The host processor can also read display module status information. Command Mode operation requires a bidirectional interface.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. Some Video Mode architectures may include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to be shut down to reduce power consumption. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

Configuration:

Lane Pair	MCU (Master) Display Module (Slave)
Clock Lane	Unidirectional Lane ■ Clock Only ■ Escape Mode(ULPS Only)
Data Lane 0	Bi-directional Lane ■ Forward High-Speed ■ Bi-directional Escape Mode ■ Bi-directional LPDT
Data Lane 1	Unidirectional Lane ■ Forward High-Speed ■ Escape Mode (ULPM only) ■ No LPDT

8.7.1 Display Module Pin Configuration for DSI



8.7.2 Display Serial Interface (DSI)

8.7.2.1 General description

The communication can be separated 2 different levels between the MCU and the display module:

- Interface Level : Low level communication

- Packet level : High level communication

8.7.2.2 Interface level communication

8.7.2.2.1 General

The display module uses data and clock lane differential pairs for DSI . Both clock lane and data lane0 can be driven Low Power (LP) or High Speed (HS) mode. Data lane1 and Data lane2 can be driven High Speed mode only.

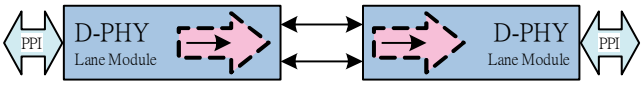
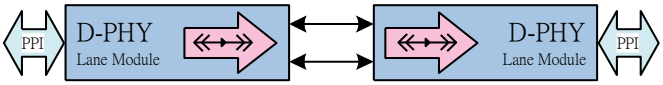
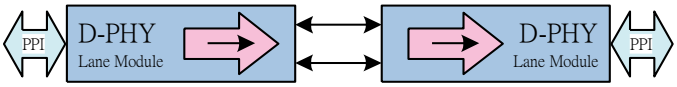
	Lane support mode	
Clock Lane	Unidirectional lane High-Speed Clock only Simplified Escape Mode (ULPS Only)	
Data Lane0	Bi-directional lane Forward high-speed only Bi-directional Escape Mode Bi-direction LPDT	
Data Lane 1	Unidirectional lane Forward high-speed only Simplified Escape Mode(ULPS Only)	

Table 13 The interface color Lane types and support mode

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State Code	Line DC voltage Levels		High Speed(HS)	Low-Power(LP)	
	Dn+ Line	Dn- Line	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Table 14 High Speed and Low-Power Lane Pair State Descriptions

Notes:

1. Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.

2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

8.7.2.2.2 DSI-CLK Lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM LP-11), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM).

Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode(LPM) or Ultra Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

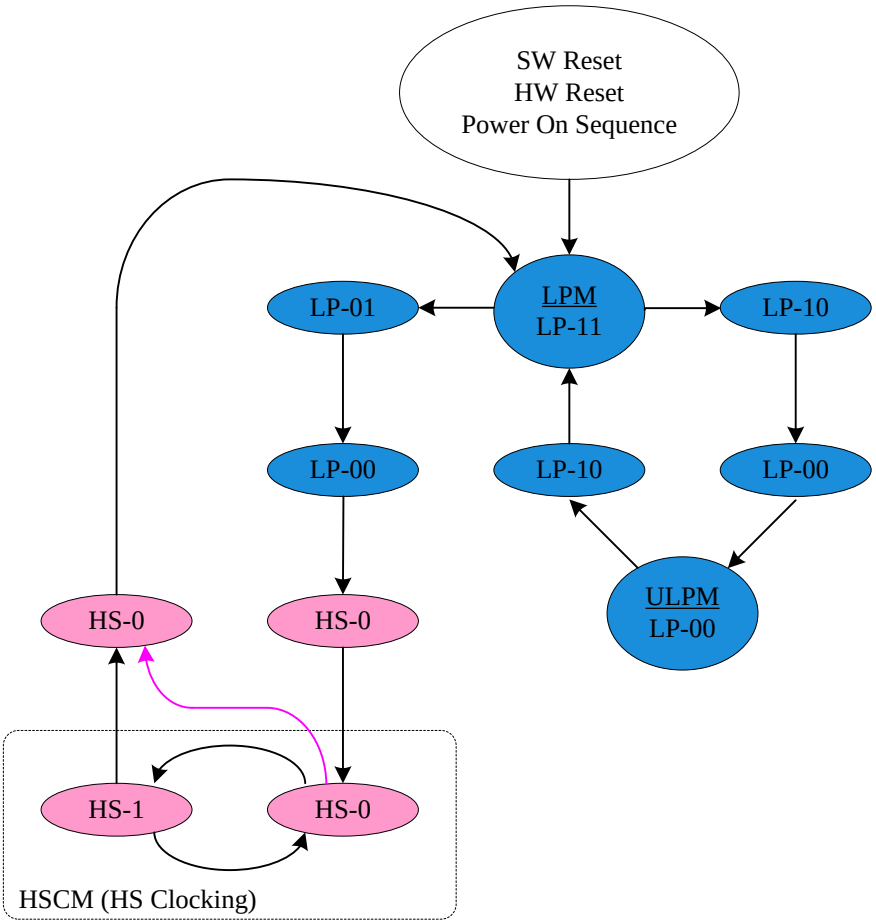


Figure 25 Clock Lanes Power Modes

8.7.2.2.1 Low Power Mode (LPM)

DSI-CLK+/- lanes can be driven to the Low Power Mode(LMP),when DSI-CLK lanes are entering LP-11 State Code , in three different ways:

After SW Reset,HW Reset or Power On Sequence=>LP-11

After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM,LP-00 State Code)=>LP10=>LP-11(LPM).

This sequence is illustrated below.

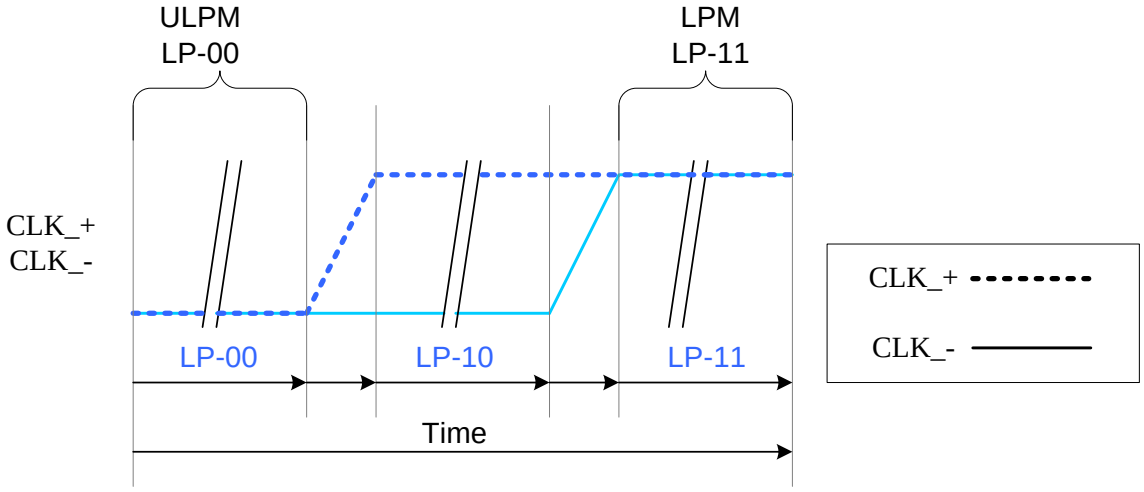


Figure 26 From ULPM to LPM

After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM).

This sequence is illustrated below.

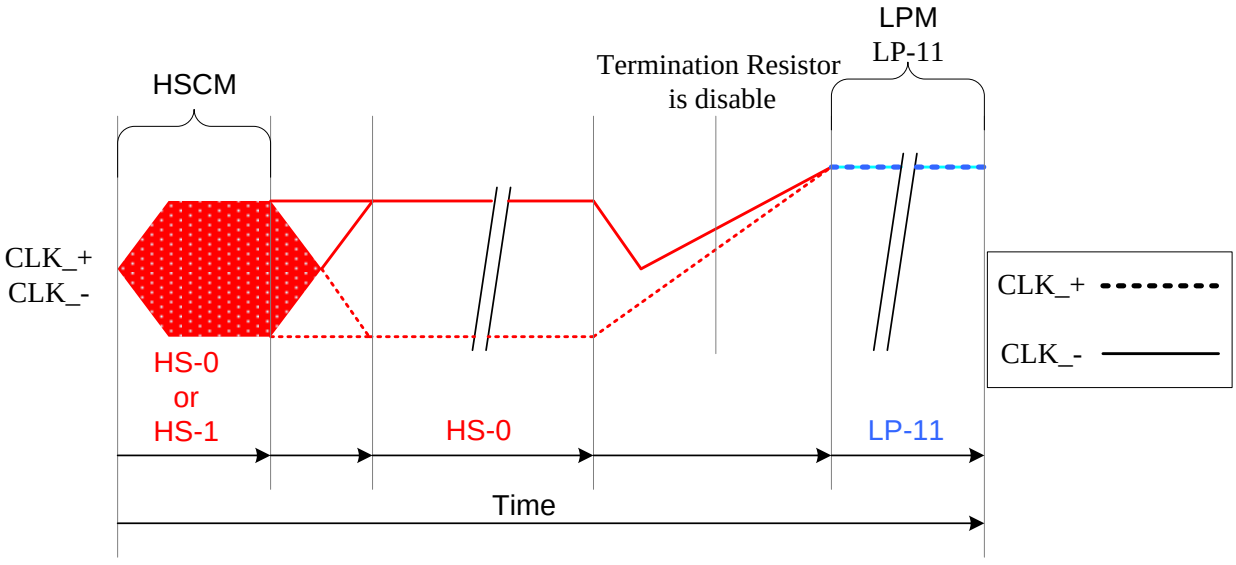


Figure 27 From HSCM to LPM

All three mode changes are illustrated a flow chart below.

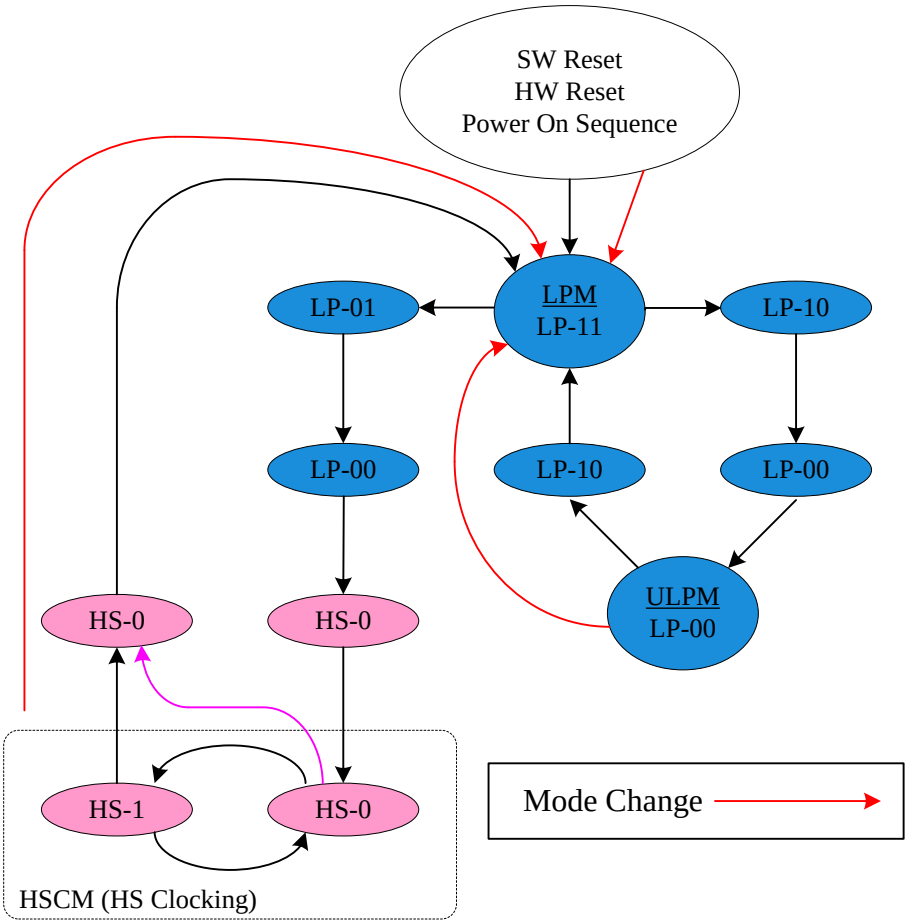


Figure 28 All three mode changes to LPM

8.7.2.2.2.2 Ultra Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the Ultra Low power Mode (ULPM), when DSI-CLK lanes are entering LP-00 State Code.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-10 =>LP-00(ULPM). This sequence is illustrated below.

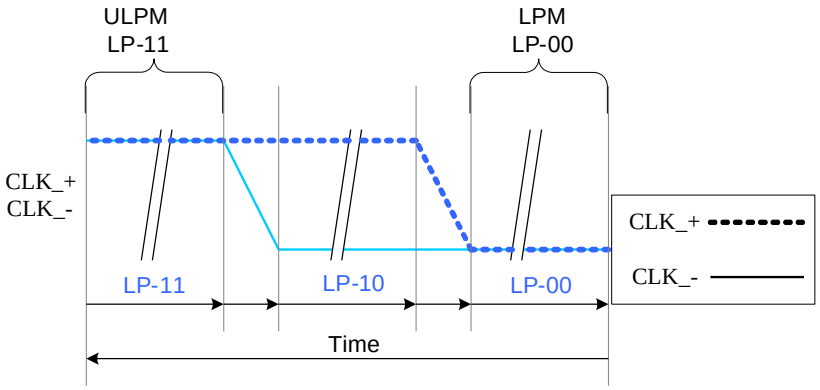


Figure 29 From LPM to UPLM

The mode change is also illustrated below:

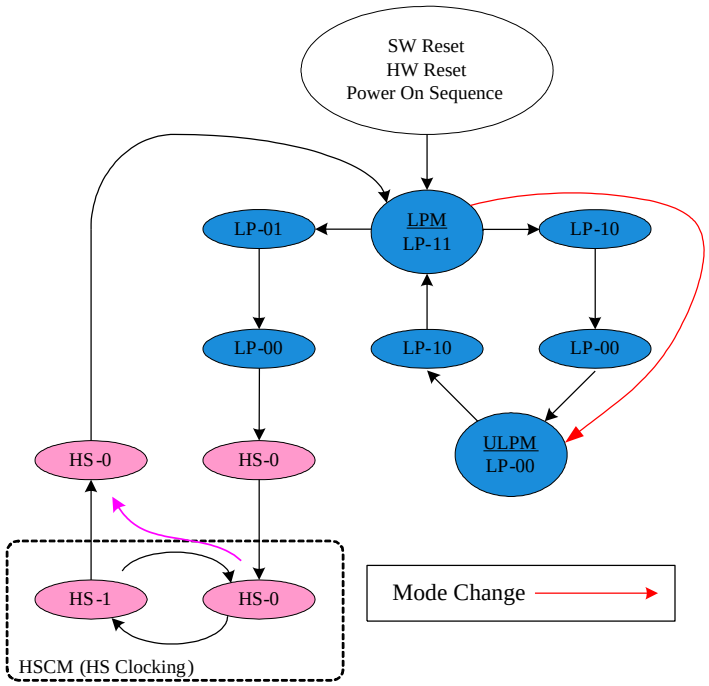


Figure 30 The mode change from LPM to UPLM

8.7.2.2.2.3 High-speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM).

This sequence is illustrated below.

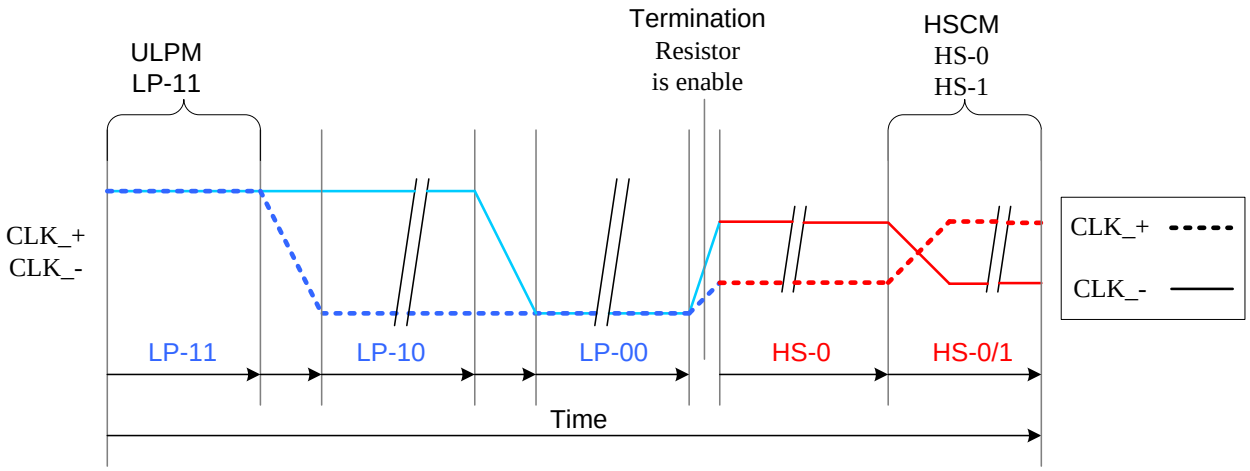


Figure 31 From LPM to HSCM

The mode change is also illustrated below:

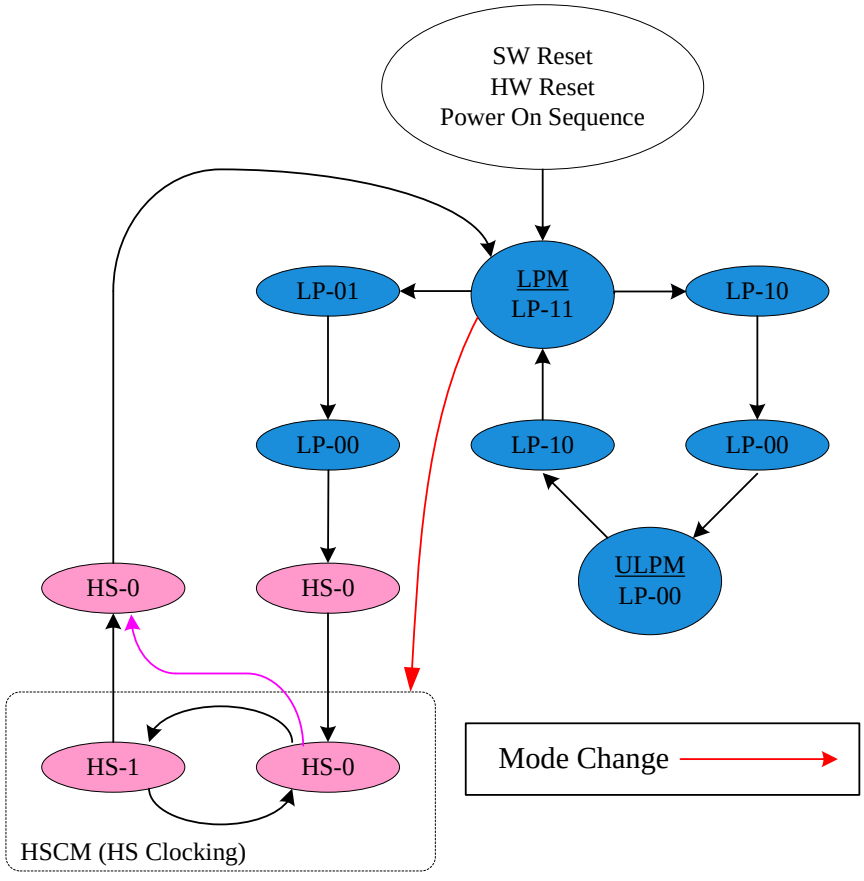


Figure 32 Mode Change from LPM to HSCM on the Flow Chart

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-Dn+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped.

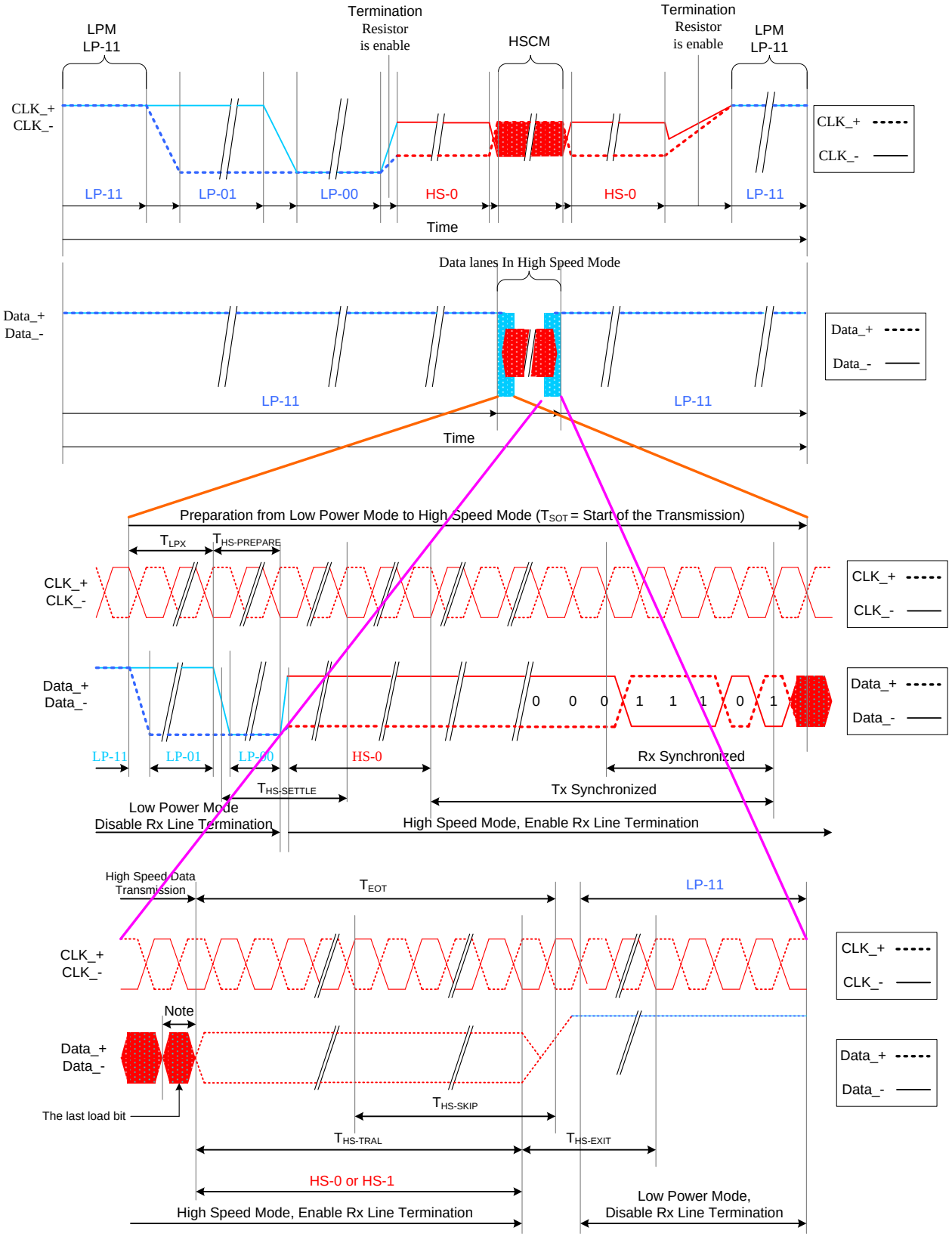


Figure 33 High Speed Clock Burst

8.7.2.2.3 DSI-DATA LANES

8.7.2.2.3.1 GENERAL

DSI-D0+/- Data Lanes can be driven in different modes which are:

• Escape Mode (Only DSI-D0+/- data lanes are used)

• High-Speed Data Transmission (DSI-D1+/- and DSI-D0+/- data lanes are used)

• Bus Turnaround Request (Only DSI-D0+/- data lanes are used)

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11=>LP-10=>LP-00=>LP-01=>LP-00	LP-00=>LP-10=>LP11(Mark1)
High-Speed Data Transmission	LP-11=>LP-01=>LP-00=>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11=>LP-10=>LP-00=>LP-10=>LP-00	High-Z

Notes:

1. Only DSI-D0+/- data lanes are used.

2. DSI-D1+/- and DSI-D0+/- data lanes are used.

3. More information on section "Bus Turnaround (BTA)"

8.7.2.2.3.2 ESCAPE MODE

Data lanes (DSI-D0+/-) can be used in different Escape Modes when data lanes are in Low Power (LP) mode. These Escape Modes are used to:

• Send “Low-Power Data Transmission” (LPDT) e.g. from the MCU to the display module

• Drive data lanes to “Ultra-Low Power State” (ULPS)

• Indicate “Remote Application Reset” (RAR), which is reset the display module

• Indicate “Tearing Effect” (TEE), which is used for a TE trigger event from the display module to the MCU

• Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MCU

The basic sequence of the Escape Mode is as follow

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0- = 0) e.g. when DSI-D0- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.

• A load if it is needed

• Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11

• End: LP-11

This basic construction is illustrated below:

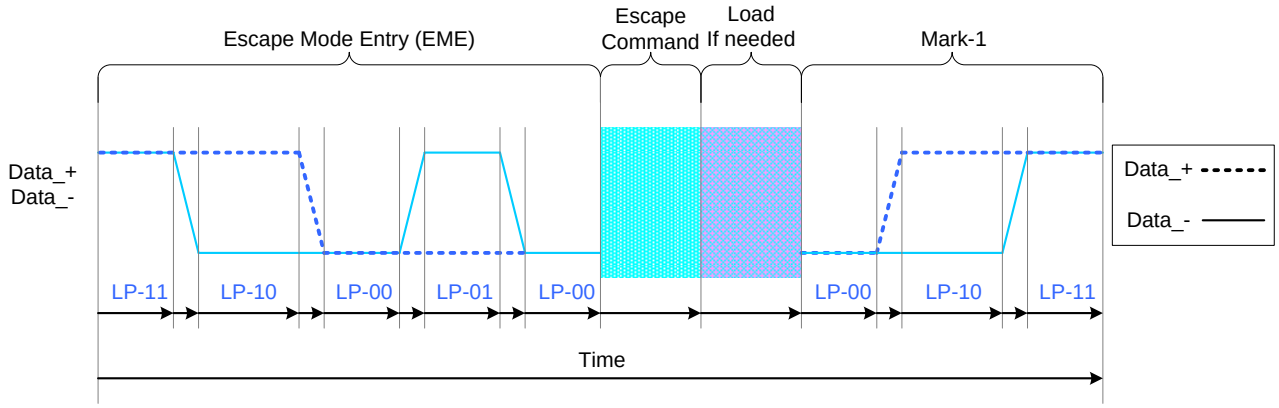


Figure 34 General Escape Mode Sequence

The number of the different Escape Commands (EC) is eight. These eight different escape commands (EC) can be divided 2 different groups: Mode or Trigger. The MCU is informing to the display module that it is controlling data lanes (DSI-D0+/-) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the low power mode. The MCU is waiting from the display module event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it.

Escape commands are defined on the next table.

This basic construction is illustrated below:

Escape Command	Command Type Mode/Trigger	Entry Command Pattern (First Bit➔Last Bit Transmitted)	Dn	D0
Low-Power Data Transmission	Mode	1110 0001 bin	-	○
Ultra-Low Power Mode	Mode	0001 1110 bin	○	○
Underfined-1, Note 1	Mode	1001 1111 bin	-	-
Underfined-2, Note 1	Mode	1101 1110 bin	-	-
Remote Application Reset	Trigger	0110 0010 bin	-	○
Tearing Effect	Trigger	0101 1101 bin	-	-
Acknowledge	Trigger	0010 0001 bin	-	○
Unknow-5,Note 1	Trigger	1010 0000 bin	-	-

Notes:

1. This Escape command support has not been implemented on the display module.

2. n=1.

3. "○"=Supported

4. "-"=Not Supported

5. Tearing Effect Trigger can not be used in MIPI Video mode.

Low-Power Data Transmission(LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

The Low Power Data Transmission (LPDT) is using a following sequence:

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)

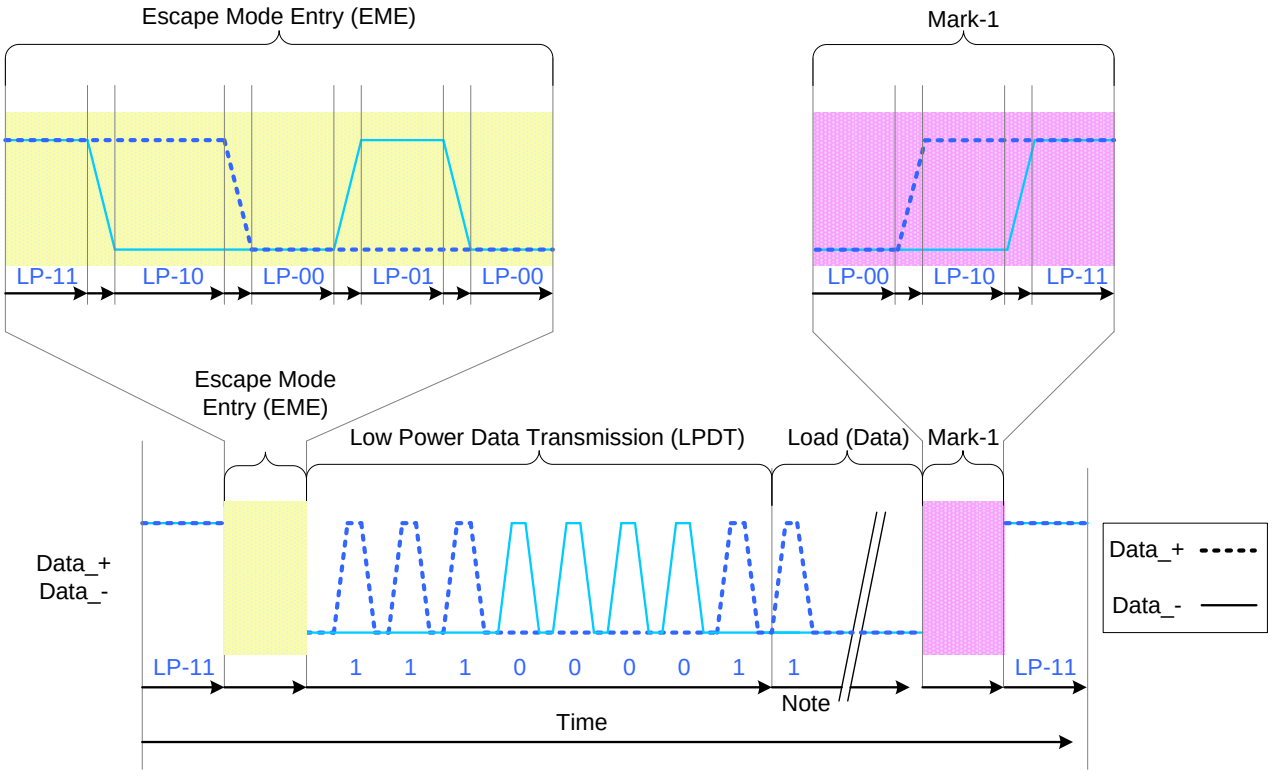
• Load (Data): One or more bytes (8 bits)

Data lanes are in pause mode when data lanes are stopped (Bothe lanes are low) between bytes

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:



Note : Load (Data) is presenting that the first bit is logical “1” in this Exsample

Figure 35 Low-Power Data Transmission (LPDT)

Notes:

Load(Data) is presenting that the first bit is logical ‘1’ in this example

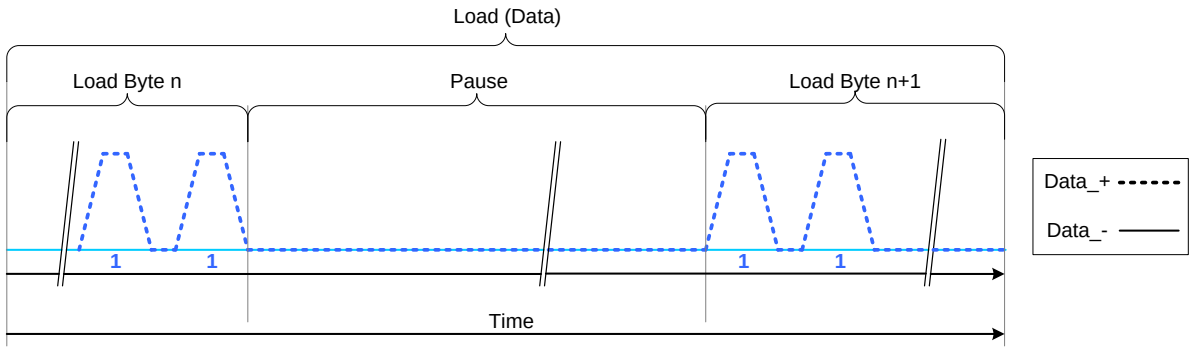


Figure 36 Pause (Example)

Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)

• Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:

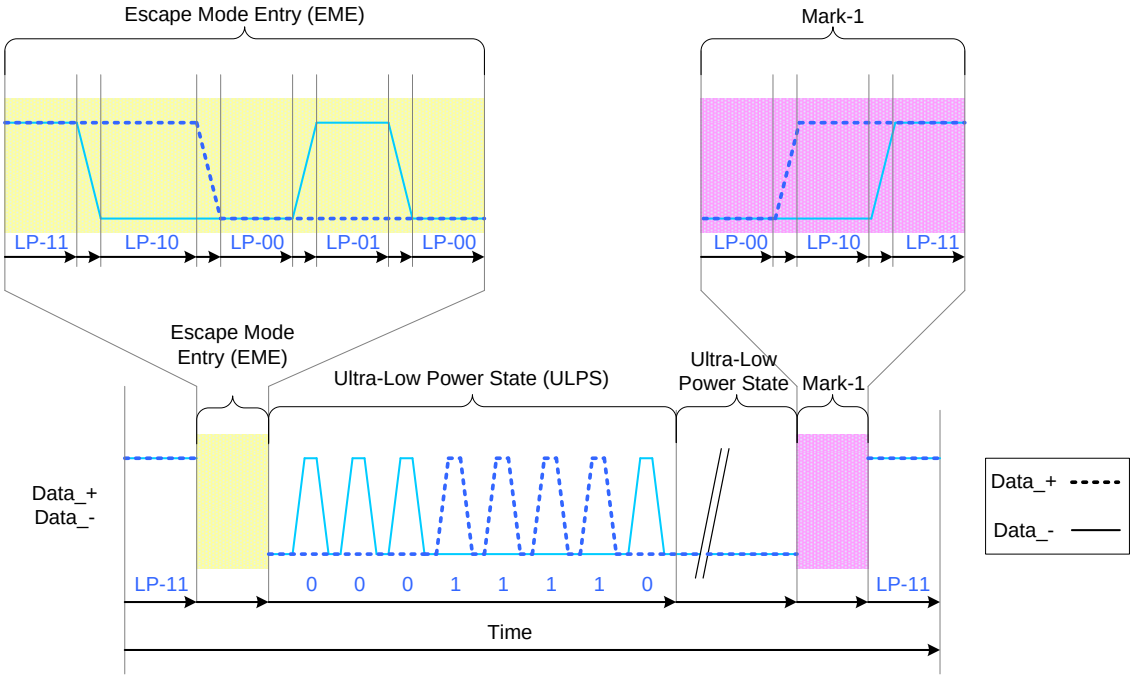


Figure 37 Ultra-Low Power State (ULPS)

Remote Application Reset (RAP)

The MCU can inform to the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:

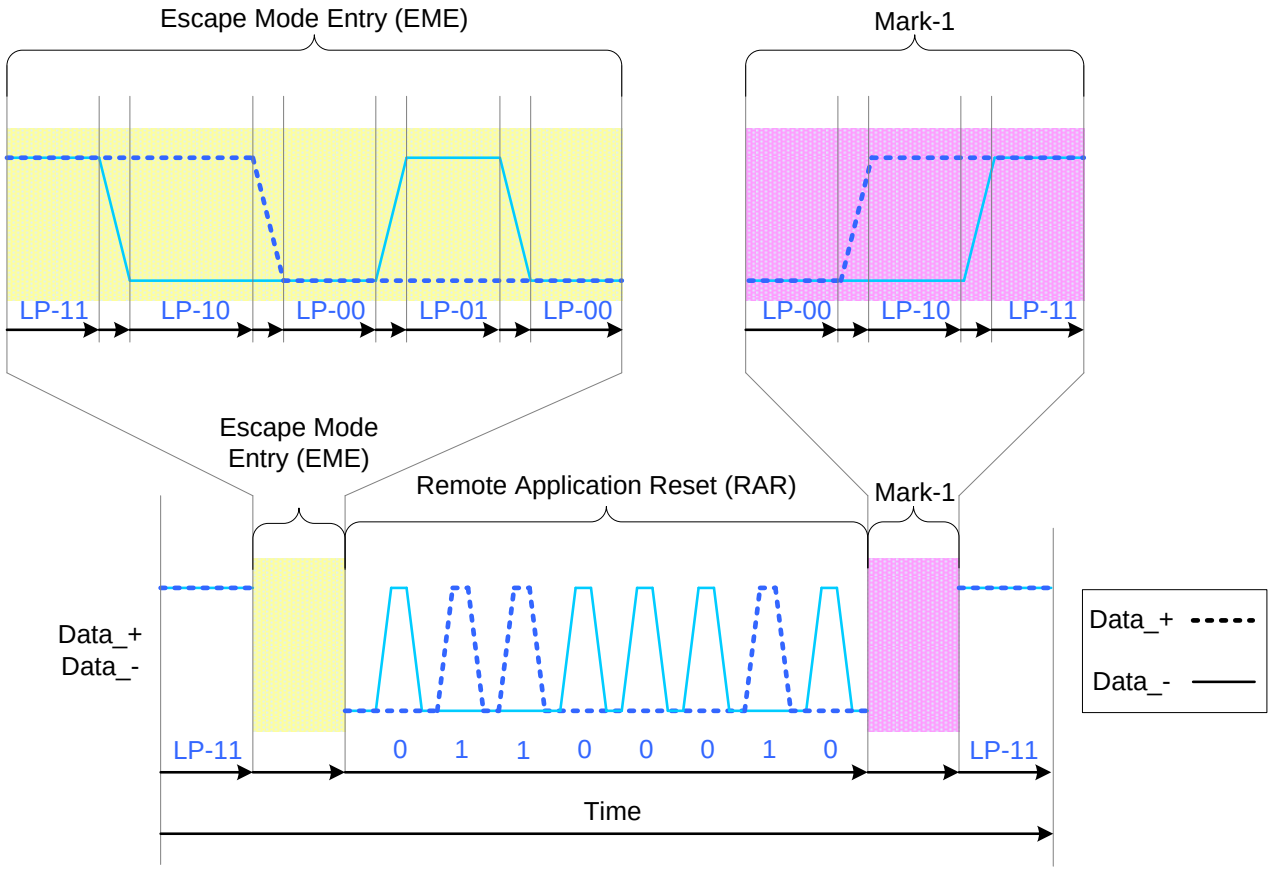


Figure 38 Remote Application Reset (RAR)

Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:

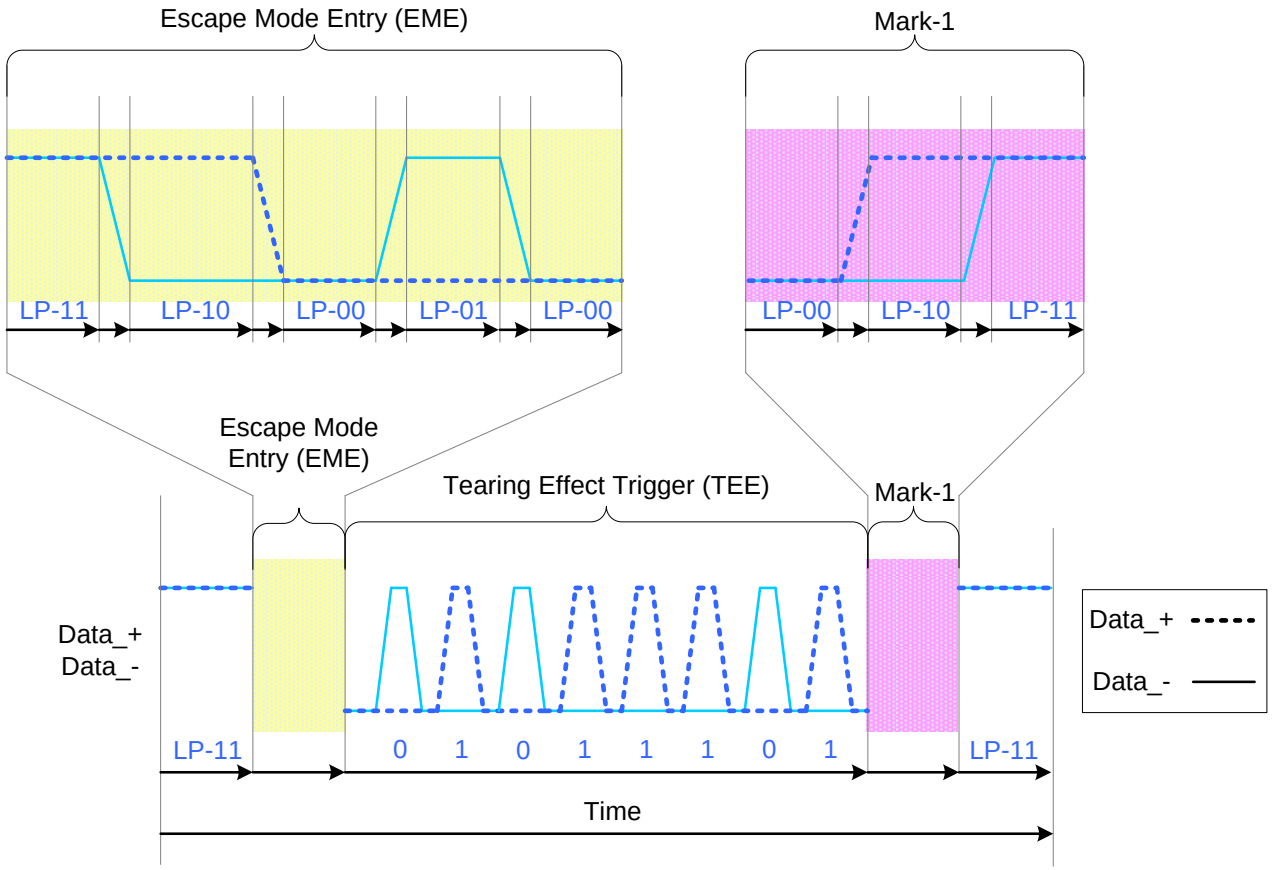


Figure 39 Tearing Effect (TEE)

Note: Tearing Effect (TEE) can not be used in MIPI Video Mode

Acknowledge (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) is using a following sequence:

• Start: LP-11

• Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:

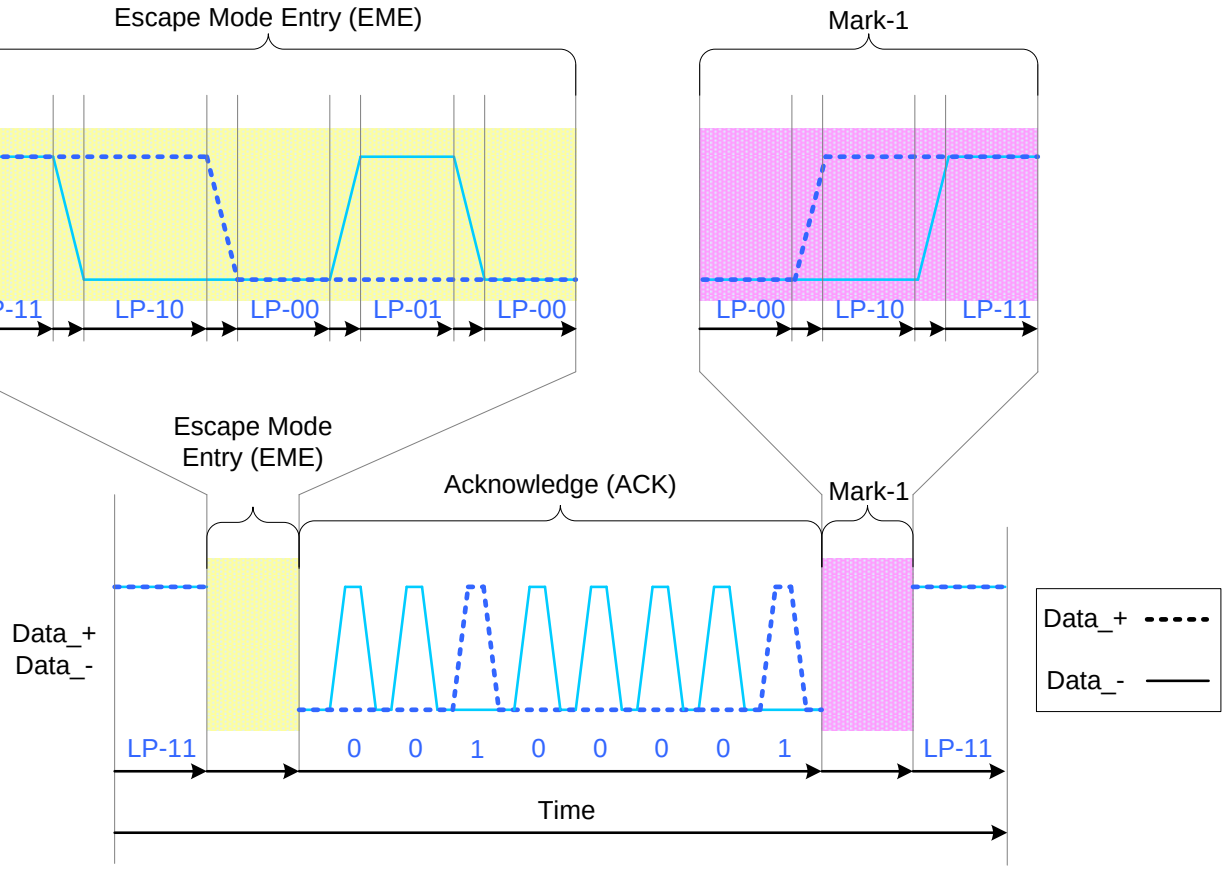


Figure 40 Acknowledge (ACK)

8.7.2.2.3.3 HIGH SPEED DATA TRANSMISSION (HSDT)

Entering High-Speed Data Transmission (T_{SOT} of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MCU. See more information on chapter "8.8.2.2.2.3 High-Speed Clock Mode (HSCM)".

Data lanes of the display module are entering (TSOT) in the High-Speed Data Transmission (HSDT) as follows

• Start: LP-11

• HS-Request: LP-01

• HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)

• Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)

• End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (TSOT of HSDT) sequence is illustrated below

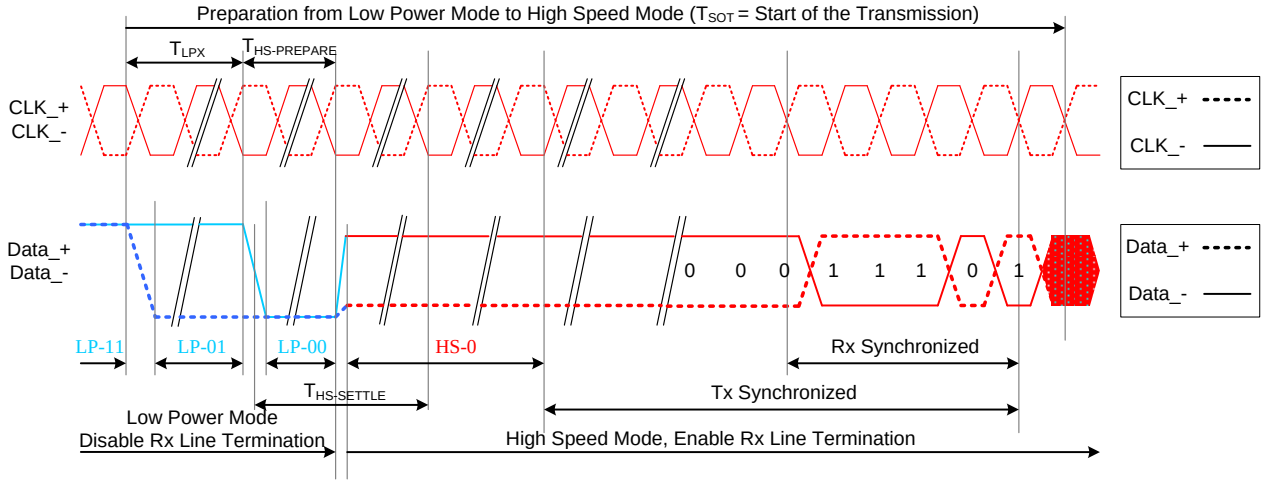


Figure 41 Entering High-Speed Data transmission (T_{SOT} of HSDT)

Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

The display module is leaving the High-Speed Data Transmission (TEOT of HSDT) when Clock lanes DSI-CLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes are in LP-11 mode. See more information on chapter “5.3.2.2.2.3 High-Speed Clock Mode (HSCM)”.

Data lanes of the display module are leaving from the High-Speed Data Transmission (TEOT of HSDT) as follows

• Start: High-Speed Data Transmission (HSDT)

• Stops High-Speed Data Transmission

• MCU changes to HS-1, if the last load bit is HS-0

• MCU changes to HS-0, if the last load bit is HS-1

• End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (TEOT of HSDT) sequence is illustrated below

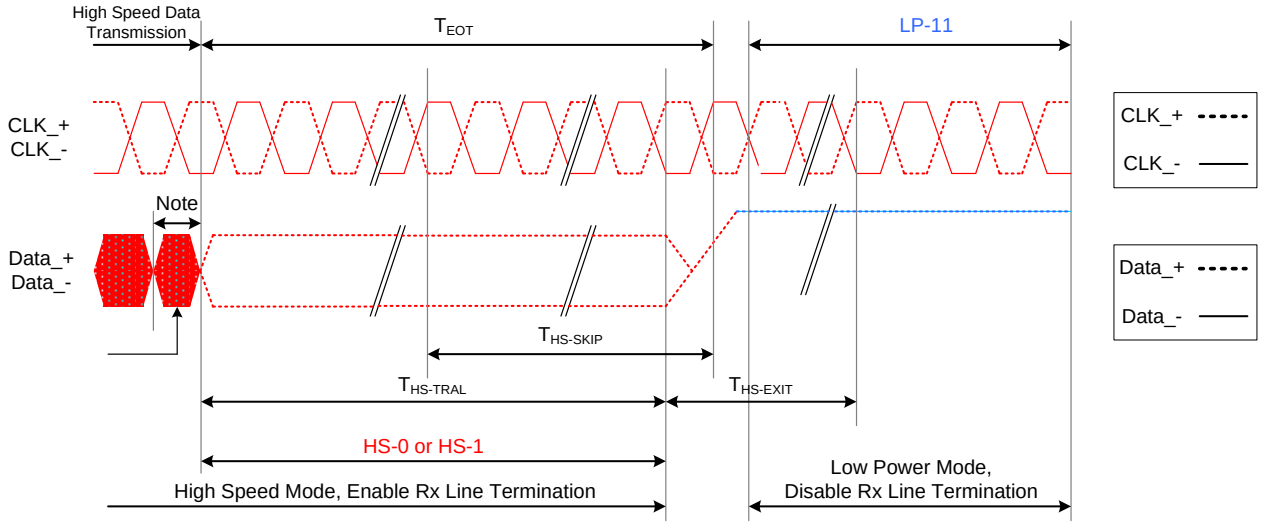


Figure 42 Levaving High-Speed data Transmission (T_{EOT} of HSDT)

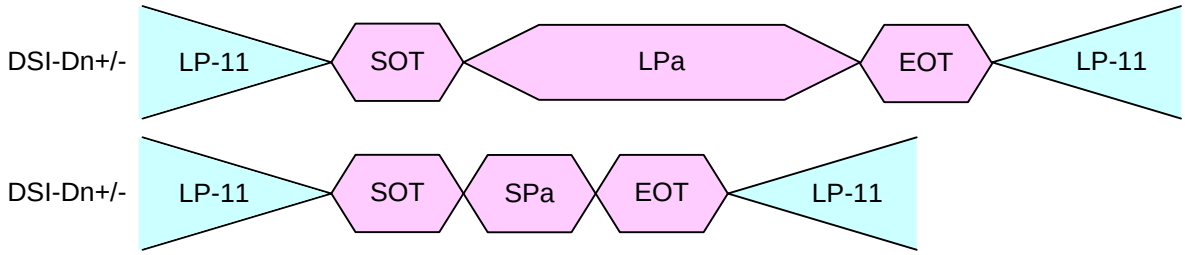
Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets.

These data packets can be Long (LPa) or Short (SPa) packets.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

Single Packet in High Speed Data Transmission



Multiple Packets in High Speed Data Transmission

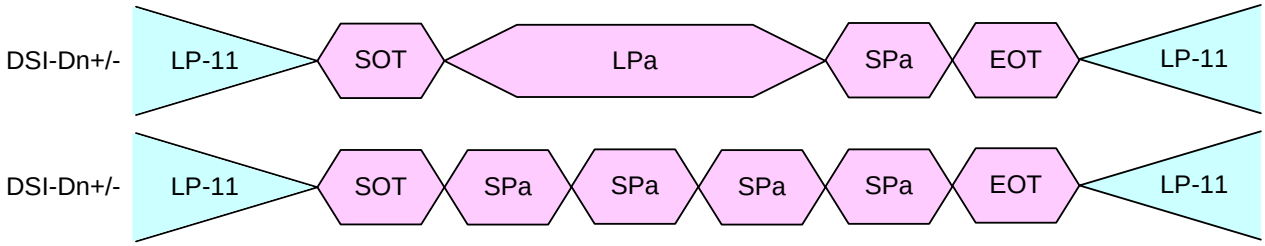
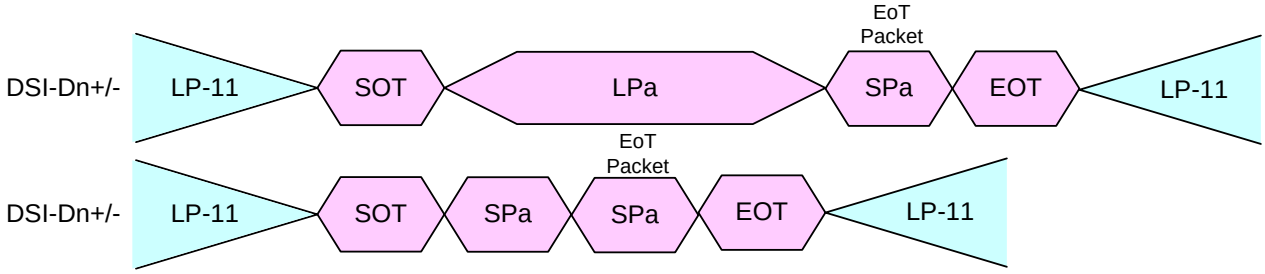


Figure 43 HS Transmission Example with EoT packet disabled

Single Packet in High Speed Data Transmission



Multiple Packets in High Speed Data Transmission

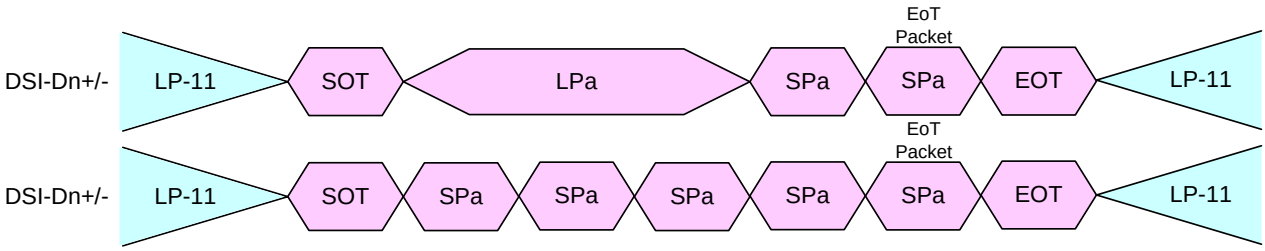


Figure 44 HS Transmission Example with EoT packet enable

Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Data lanes are’1’s (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

Bus Turnaround (BTA)

The MCU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or display module.

The MCU or display module are using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to the display module, as follow.

• Start (MCU):LP-11

• Turnaround Request (MCU): LP-11 _ LP-10 _ LP-00 _ LP-10 _ LP-00

• The MCU wait until the display module is starting to control DSI-D0+/- data lanes and the MCU stop to control DSI-D0+/- data lanes (=High-Z)

• The display module changes to the stop mode: LP-00 _ LP-10 _ LP-11

The same bus turnaround .procedure (From the MCU to the display module) is illustrated below.

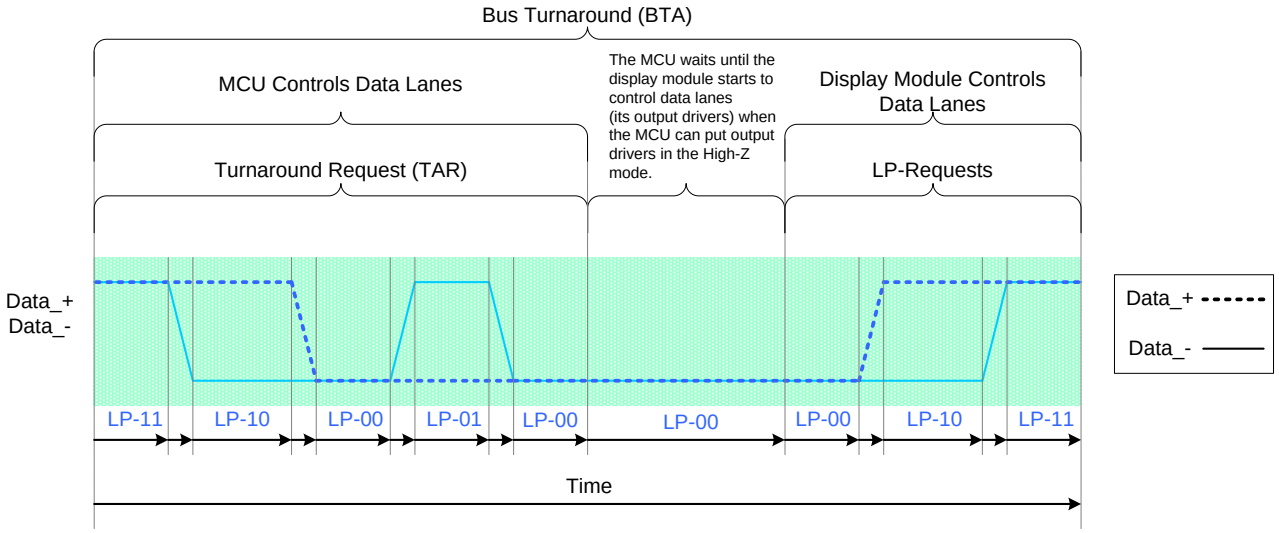


Figure 45 Bus Turnaround Procedure

MCU and the display module terms are switched on above figure, if the Bus Turnaround (BTA) is from the display module to the MCU..

8.7.2.3 Packet Level Communication

8.7.2.3.1 Short Packet (SPA) And Long Packet (LPA) Structure

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

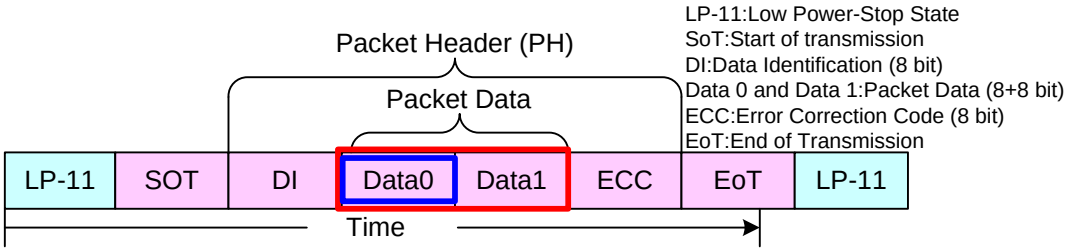
The lengths of the packets are

• Short Packet (SPa): 4 bytes

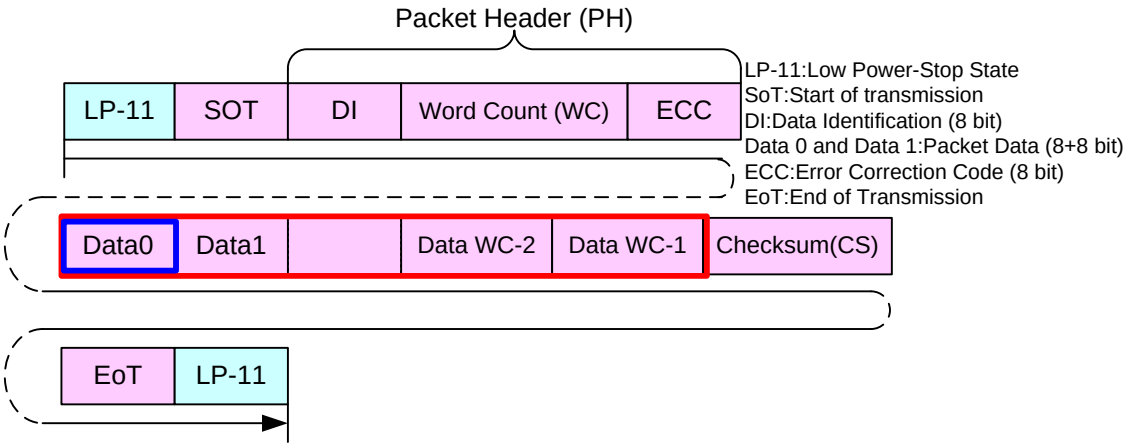
• Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

Short Packet (Spa) Structure:



Long Packet (Spa) Structure:



Note:

Short Packet (SPa) Structure and Long Packet (LPa) Structure are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sendings).

The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format e.g.

** LP-11 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-11*

** LP-11 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-11*

** LP-11 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-11*

8.7.2.3.1.1 Bit Order of the Byte on Packets

The bit order of the byte, what is used on packets, is that the Least Significant Bit (LSB) of the byte is sent in the first and the Most Significant Bit (MSB) of the byte is sent in the last.

This same order is illustrated for reference purposes below.

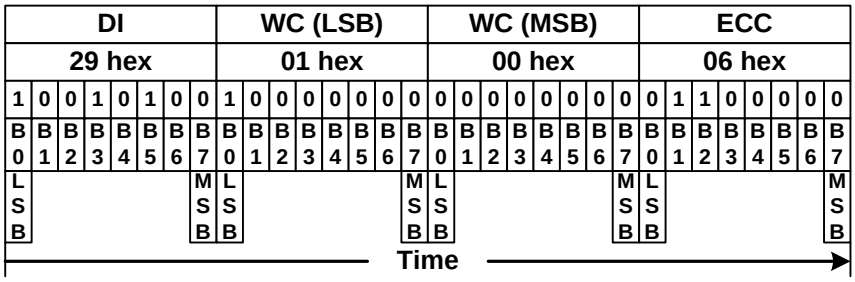


Figure 46 Bit Order of Byte on Packets

8.7.2.3.1.2 Bit Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.

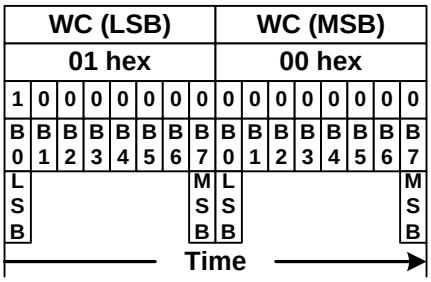


Figure 47 Byte Order of the Multiple Byte on Packets

8.7.2.3.1.3 Pack Header (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

• 1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)

• 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1

• 4th byte: Error Correction Code (ECC)

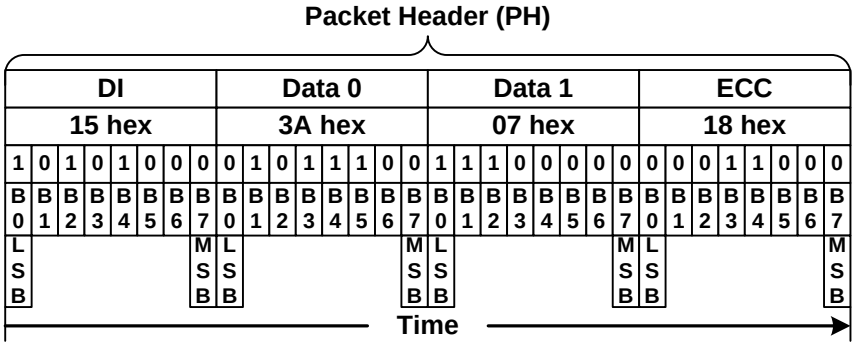


Figure 48 Packet Header (PH) on Short Packet(Spa)

Long Packet (LPa):

• 1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)

• 2nd and 3rd bytes: Word Count (WC)

• 4th byte: Error Correction Code (ECC)

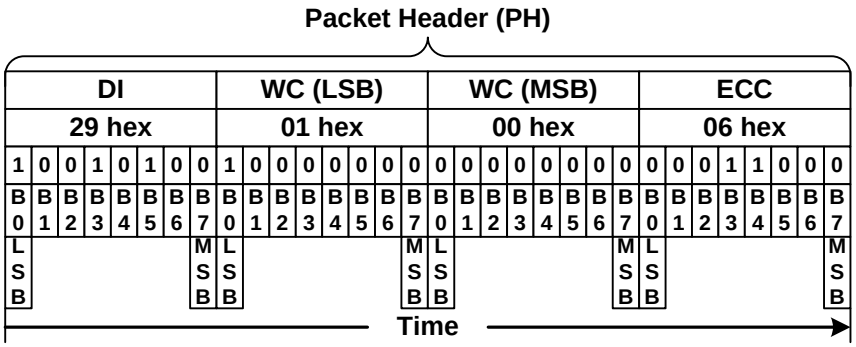


Figure 49 Packet Header (PH) on Long Packet (LPa)

Data Identification (DI)

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

• Virtual Channel (VC), 2 bits, DI[7...6]

• Data Type (DT), 6 bits, DI[5…0]

The Data Identification (DI) structure is illustrated on a table below.

Data Identification (DI)							
Virtual Channel (VC)		Data Type (DT)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Figure 50 Data Identification (DI) Structure

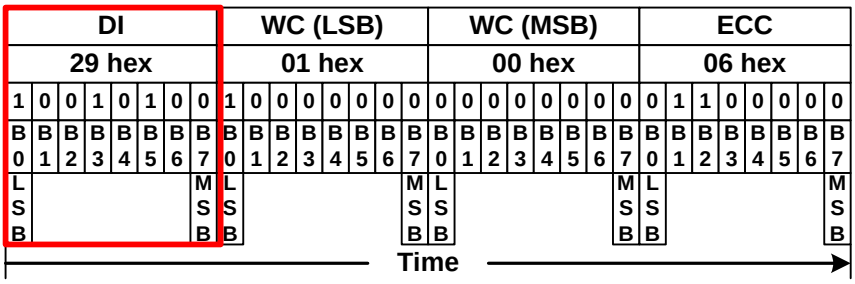


Figure 51 Data Identification (DI) on the Packet Header(PH)

Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI[7…6]) structure and it is used to address where a packet is wanted to send from the MCU.

Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

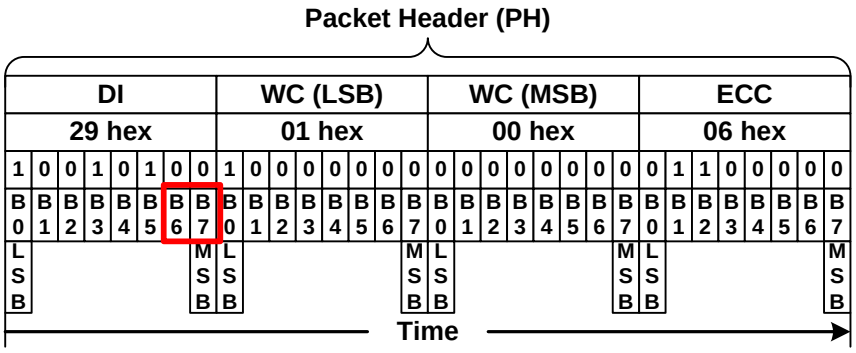


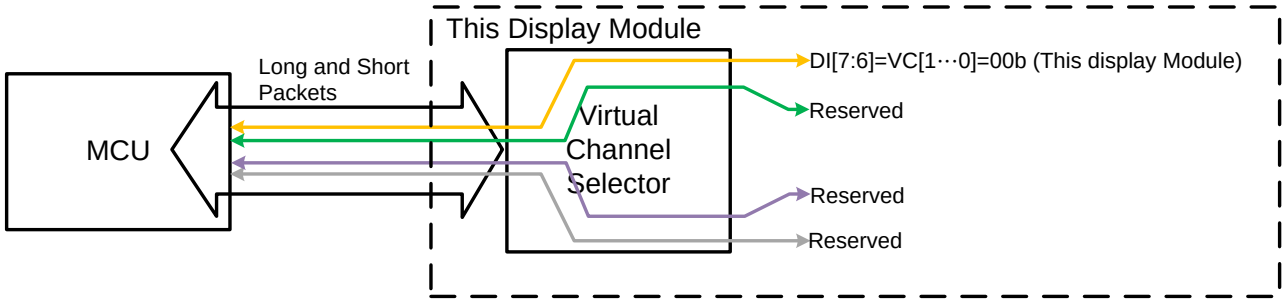
Figure 52 Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can address 4 different channels for e.g. 4 different display modules. Devices are using the same virtual channel what the MCU is using to send packets to them e.g.

• The MCU is using the virtual channel 0 when it sends packets to this display module

• This display module is also using the virtual channel 0 when it sends packets to the MCU

This functionality is illustrated below.



Virtual Channel (VC) Configuration

Virtual Channel (VC) always 0 (D[7...6]=VC[1…0]00b) when the MCU is sending “End of Transmission Packet” to the display module. See section “End of Transmission Packet (EoTP)

This display module is not supporting the virtual channel selector for other device (1 to 3) when only possible virtual channel (VC[1…0]) is 00b for this display module.

Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.

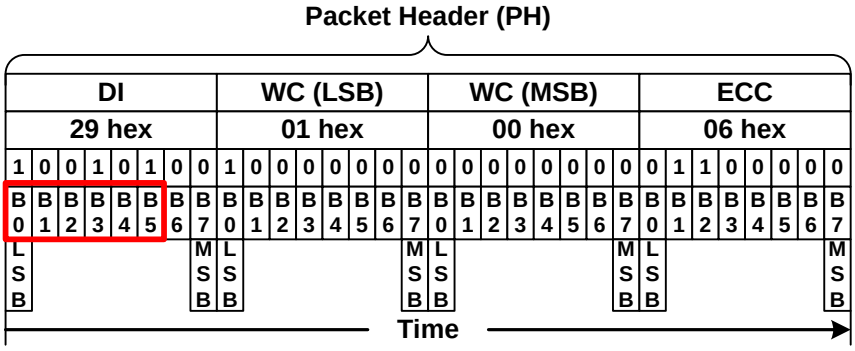


Figure 53 Data Type (DT) on the Packet Header (PH)

This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa.

These Data Type (DT) are defined on tables below.

Data Type Hex	Data Type Binary	Description	Packet Size
01h	00 0001	Sync Event, V Sync Start.	Short
11h	01 0001	Sync Event, V Sync End.	Short
21h	10 0001	Sync Event, H Sync Start.	Short
31h	11 0001	Sync Event, H Sync End.	Short
08h	00 1000	End of Transmission (EoT) packet.	Short
02h	00 0010	Color Mode (CM) Off Command.	Short
12h	01 0010	Color Mode (CM) On Command.	Short
22h	10 0010	Shut Down Peripheral Command.	Short
32h	11 0010	Turn On Peripheral Command.	Short
03h	00 0011	Generic Short WRITE, no parameters	Short
13h	01 0011	Generic Short WRITE, 1 parameter.	Short
23h	10 0011	Generic Short WRITE, 2 parameters.	Short
04h	00 0100	Generic READ, no parameters.	Short
14h	01 0100	Generic READ, 1 parameter.	Short
24h	10 0100	Generic READ, 2 parameters.	Short
05h	00 0101	DCS WRITE, no parameter.	Short
15h	01 0101	DCS WRITE, 1 parameter.	Short
06h	00 0110	DCS READ, no parameter.	Short
37h	11 0111	Set Maximum Return Packet Size.	Short
09h	00 1001	Null Packet, no data.	Long
19h	01 1001	Blanking Packet, no data.	Long
29h	10 1001	Generic Long Write.	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet.	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB,5-6-5 Format.	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB,6-6-6 Format.	Long
2Eh	10 1110	Loosely Packed Pixel Stream,18-bit RGB,6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream,24-bit RGB,8-8-8 Format.	Long

Table 15 Data Type (DT) from MCU to the Display Module (or Other Devices)

From the Display Module (or Other Devices) to the MCU									
Hex	B5	B4	B3	B2	B1	B0	Description	Packet	Abbreviation
02h	0	0	0	0	1	0	Acknowledge with Error Report	Short	AwER
1Ch	0	1	1	1	0	0	DCS Read Long Response	Short	DCSRR_L
21h	1	0	0	0	0	1	DCS Read Short Response, 1 byte returned	Short	DCSRR1_S
22h	1	0	0	0	1	0	DCS Read Short Response, 2 byte returned	Short	DCSRR2_S
1Ah	0	1	1	0	1	0	Generic Read Long Response	Short	GENRR-L
11h	0	1	0	0	0	1	Generic Read Short Response,1 byte returned	Short	GENRR1-S
12h	0	1	0	0	1	0	Generic Read Short Response,2 byte returned	Short	GENRR2-S

Table 16 Data Type (DT) from the Display Module (or Other Devices) to the MCU

The receiver will ignore other Data Type (DT) if they are not defined on tables: “Data Type (DT) from the MCU to the Display Module (or Other Devices)” or “ Data Type (DT) from the Display Module (or Other Devices) to the MCU”.

Packet Data (PD) on the Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send.

The Word Count (WC) indicates the number of Bytes of Packet of Packet Data (PD) send after the Packet Header.

Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last.

Bits of Data 1 are set to '0' if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below, when Virtual Channel (VC) is 0.

Packet Data (PD) information:

• Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI(Data Type (DT)) = 15hex)

• Data 1: 01hex (DCS's parameter)

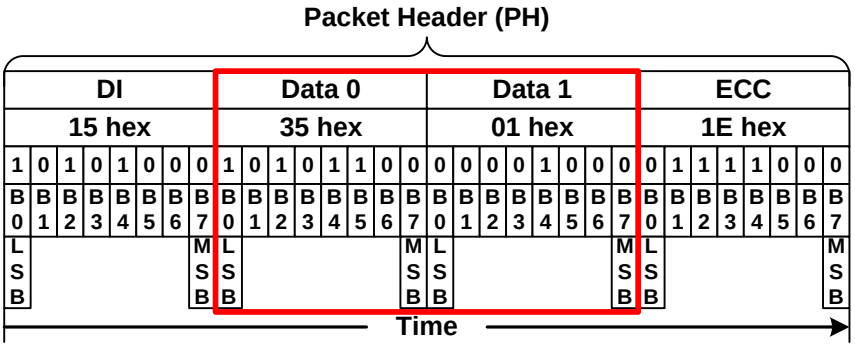


Figure 54 Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

Packet Data (PD) information:

• Data 0: 10hex (DCS without parameter => DI(Data Type (DT)) = 05hex)

• Data 1: 00hex (Null)

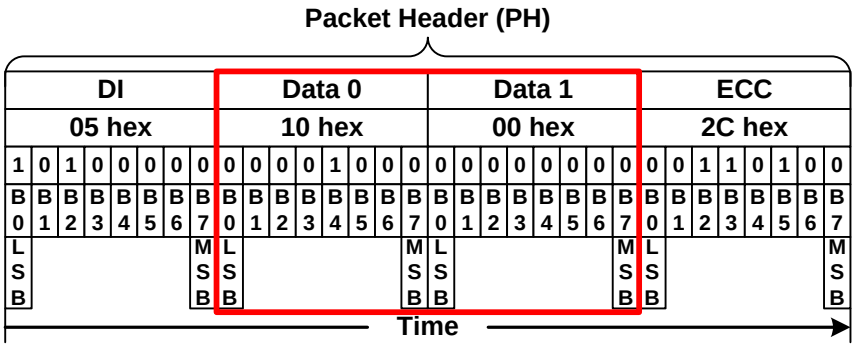


Figure 55 Packet Data(PD) fo Short Packet (Spa), 1 Bytes Information

Word Count (WC) on the Long Packet (LPa)

Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LPa) is wanted to send.

Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH).

Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.

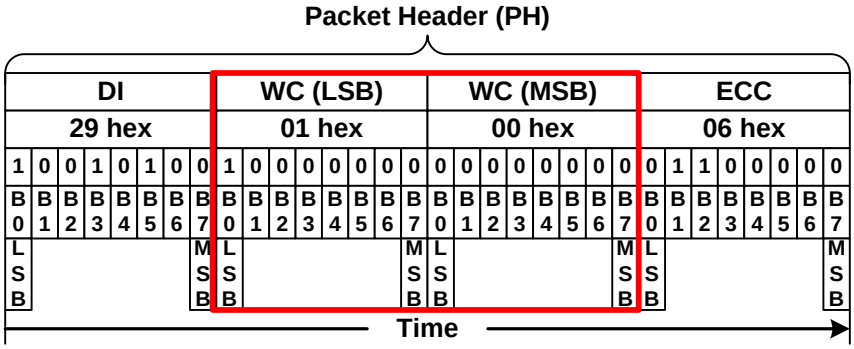
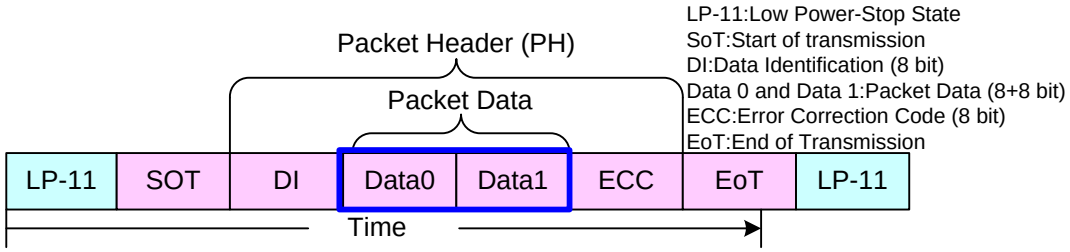
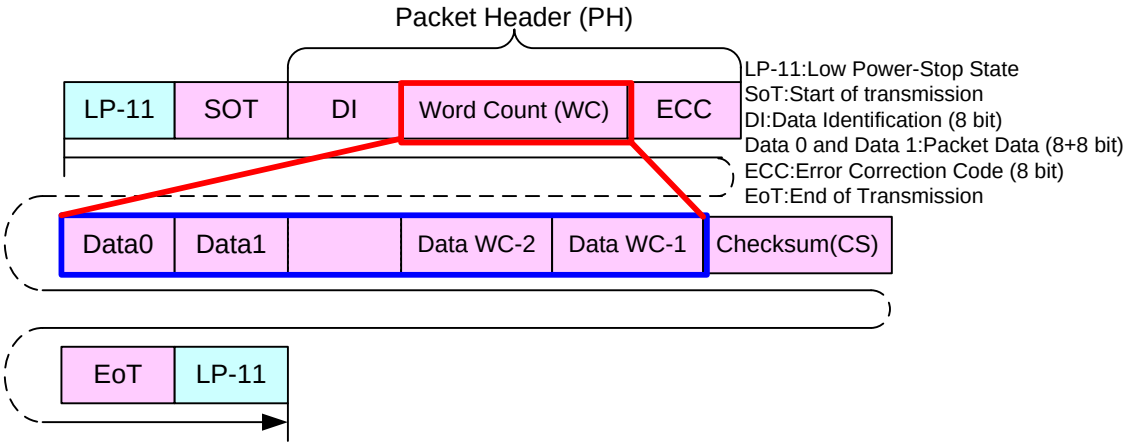


Figure 56 Word Count (WC) on the Long Packet (LPa)

Short Packet:



Long Packet:



Error Correction Code (ECC)

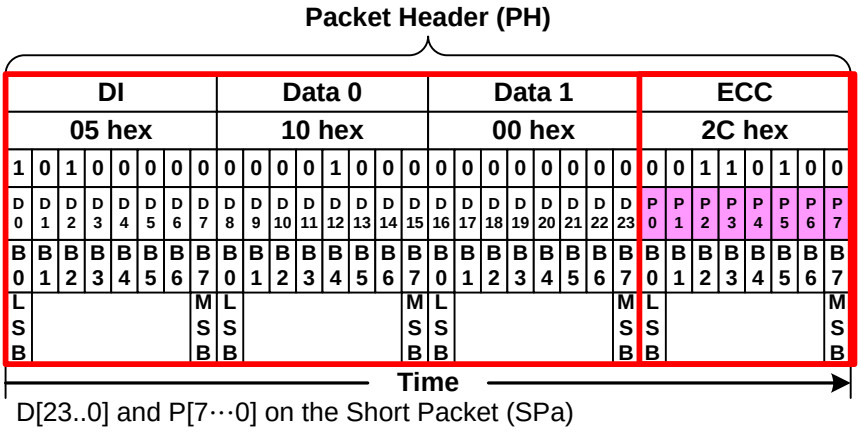
Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors on the Packet Header (PH):

The ECC protects the following field"

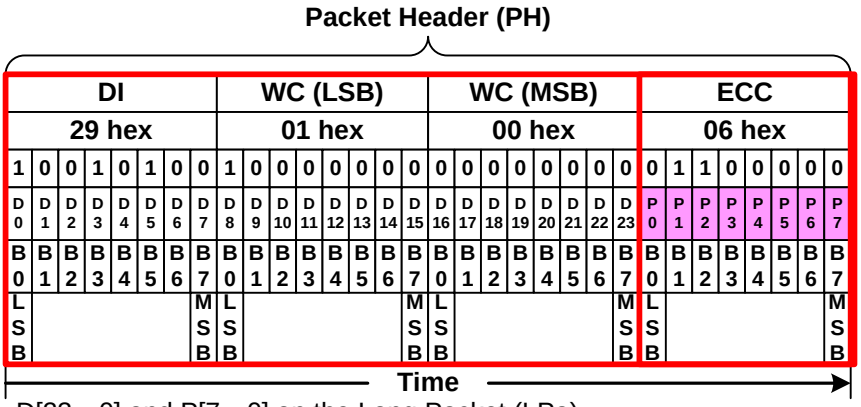
• Short Packet (SPa): Data Identification (DI) byte (8 bits, D[0...7]), Packet Data (PD) bytes (16 bits, D[8...23]) and ECC(8 bits: P[0…7])

• Long Packet (LPa): Data Identification (DI) byte (8 bits, D[0…7]), Word Count (WC) bytes (16 bits: D[8…23]) and ECC (8 bits, P[0…7])

D[23…0] and P[7…0] are illustrated for reference purposes below.



D[23..0] and P[7⋯0] on the Short Packet (SPa)



D[23⋯0] and P[7⋯0] on the Long Packet (LPa)

Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

• P7 = 0

• P6 = 0

• P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

• P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

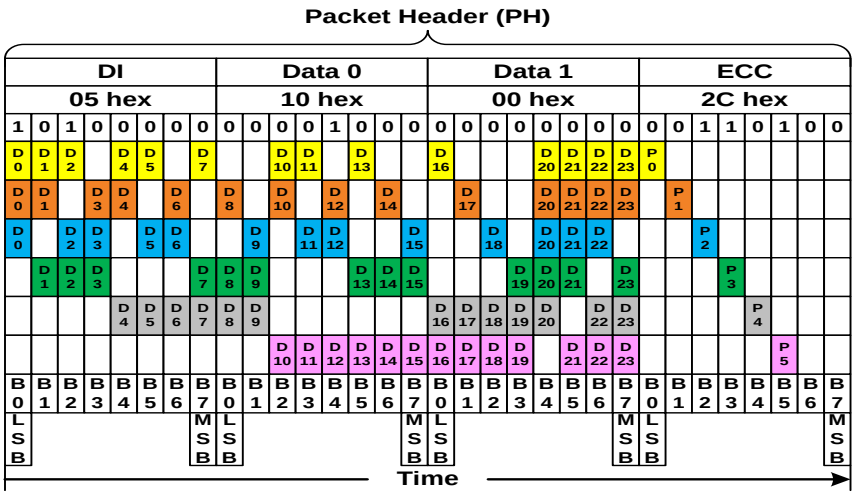
• P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

• P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

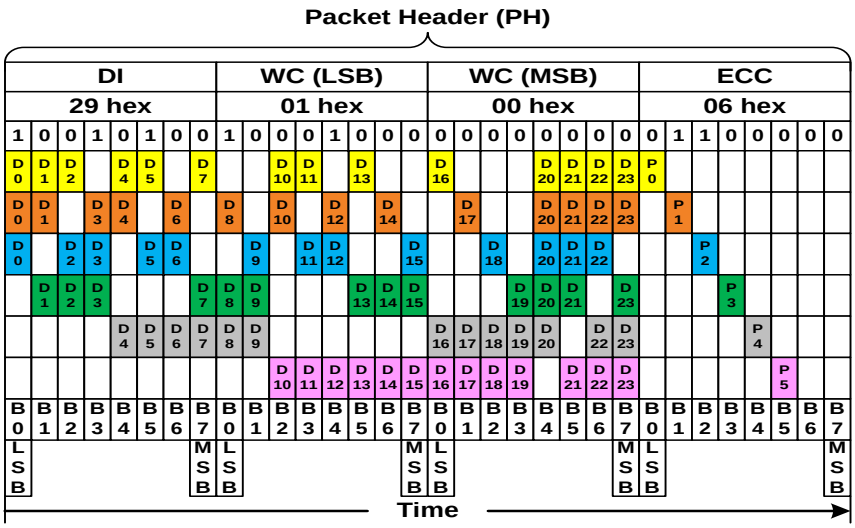
• P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

• P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D[23…0]). Therefore, there is only needed 6 bits (P[5…0]) for Error Correction Code (ECC).



XOR Functionality on the Short Packet (SPa)



XOR Functionality on the Long Packet (LPa)

The transmitter (The MCU or the Display Module) is sending data bits D[23…0] and Error Correction Code (ECC) P[7…0]. The receiver (The Display module or the MCU) is calculate an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO[7…0].

This functionality, where the transmitter is the MCU and the receiver is the display module, is illustrated for reference purposes below.

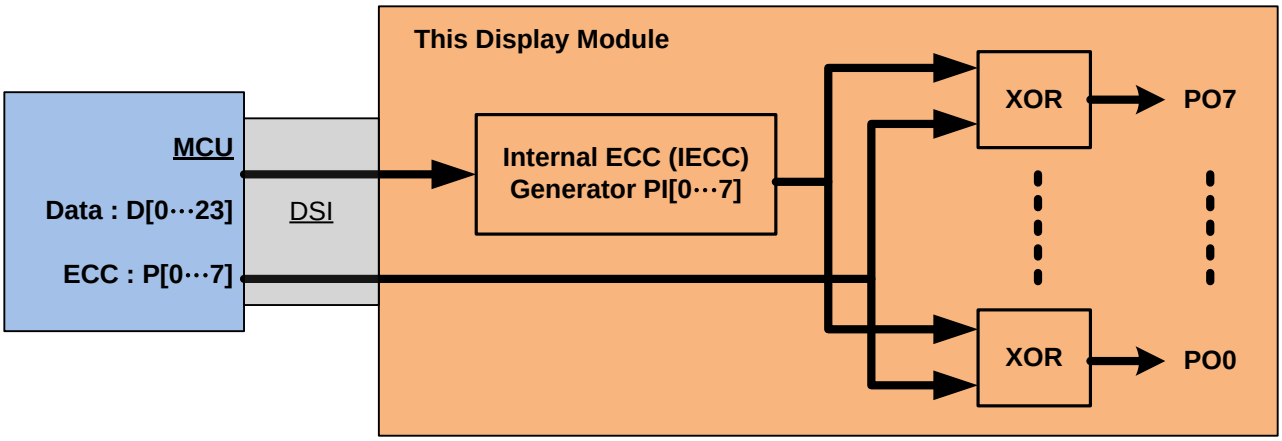


Figure 57 Internal Error Correction Code (IECC) on the Display Module (The Receiver)

The sent data bits (D[23…0]) and ECC (P[7…0]) are received correctly, if a value of the PO[7…0]) is 00h. The sent data bits (D[23…0]) and ECC (P[7…0]) are not received correctly, if a value of the PO[7…0]) is not 00h.

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	0	0	0	0	0	0	03h
XOR(ECC,IECC) =>PO[7…0]	0	0	0	0	0	0	0	0	=00h=>No Error
	L							M	
	S							S	
	B							B	

Internal XOR Calculation between ECC and IECC Values-No Error

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC,IECC) =>PO[7…0]	0	0	1	1	0	0	0	0	=0Ch=> Error
	L							M	
	S							S	
	B							B	

Internal XOR Calculation between ECC and IECC Values- Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D[23…0] on the transmitter side.

The number of the errors (one or more) can be defined when the value of the PO[7…0] is compared to values on the following table.

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

One error is detected if the value of the PO[7…0] is on : One Bit Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

• PO[7…0] = 0Eh

• The bit of the data (D[23…0]), what is not correct, is D[3]

More than one error is detected if the value of the PO[7…0] is not on: One Bit Error Value of the Error Correction Code (ECC) e.g. PO[7…0] = 0Ch.

8.7.2.3.1.4 Packet Data (PD) on the Long Packet (LPa)

Packet Data (PD) of the Long Packet (LPa) is defined after Packet Header (PH) of the Long Packet (LPa). The number of the data bytes is defined on chapter “Word Count (WC) on the Long Packet (LPa)”.

8.7.2.3.1.5 Packet Footer (PF) on the Long Packet (LPa)

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa).

The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial X16+X12+X5+X0 as it is illustrated below.

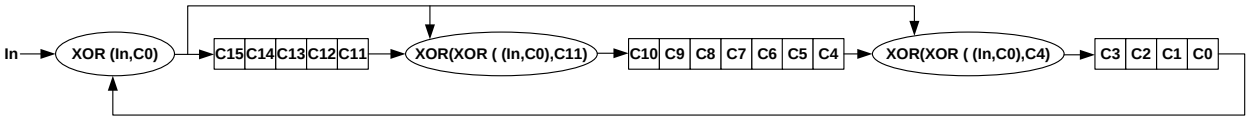
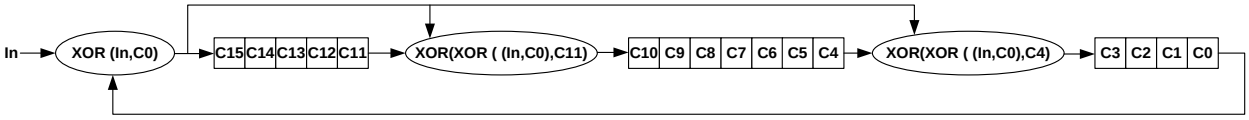


Figure 58 16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Least Significant Bit (LSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.



Stop	In	XOR(In,C0)	C15	C14	C13	C12	C11	XOR(XOR(In,C0),C11(Step-1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR(In,C0),C4(Step-1))	C3	C2	C1	C0	C0
0	X	X	1	1	1	1	1	X	1	1	1	1	1	1	1	X	1	1	1	1	X
1	1(LSB)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
5	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
6	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0
7	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0
8	0(MSB)	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
	1 Byte	CRC Resoult	0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0	
			LSB																	LSB	

Figure 59 CRC Calculation – Packet Data (PD) is 01h

A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is illustrated below.

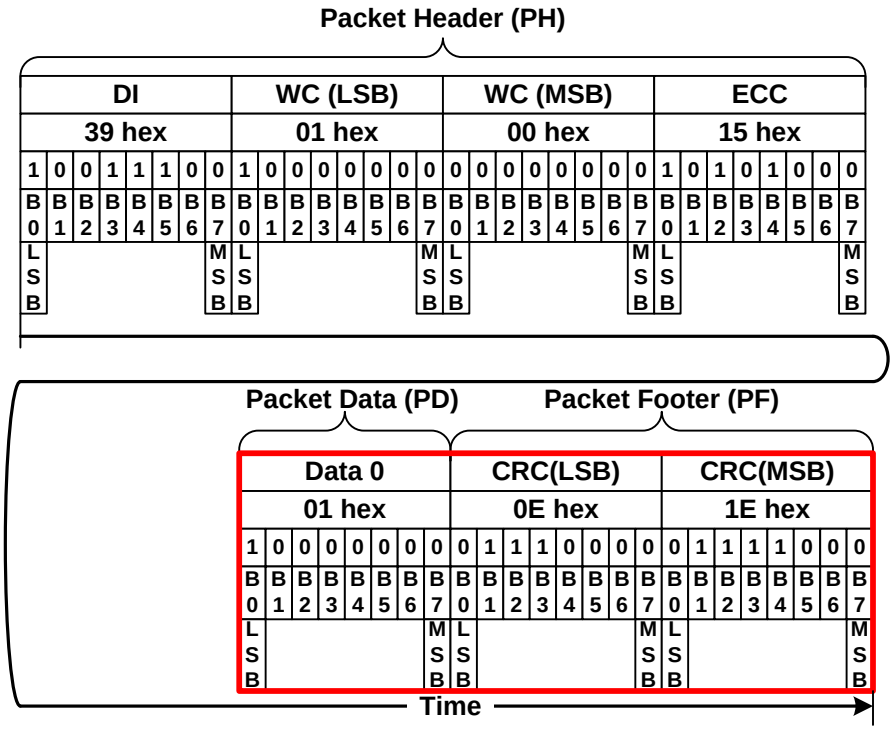


Figure 60 Packet Footer (PF) Example

The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

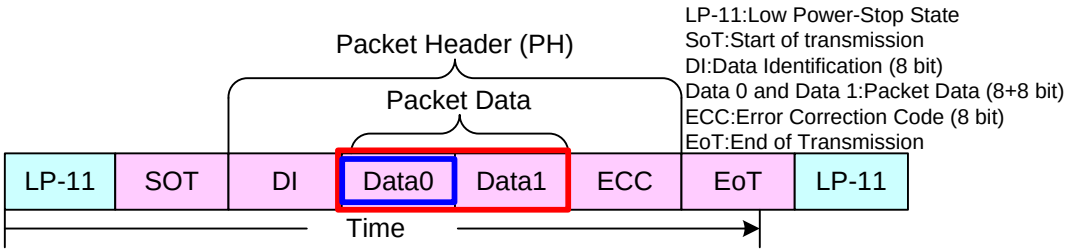
8.7.2.3.2 Packet Transmissions

8.7.2.3.2.1 Packet from the MCU to the Display Module

Display Command Set (DCS)

Display Command Set (DCS), which is defined on chapter “9 Instruction Description”, is used from the MCU to the display module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD),which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated below.

Short Packet



Long Packet:

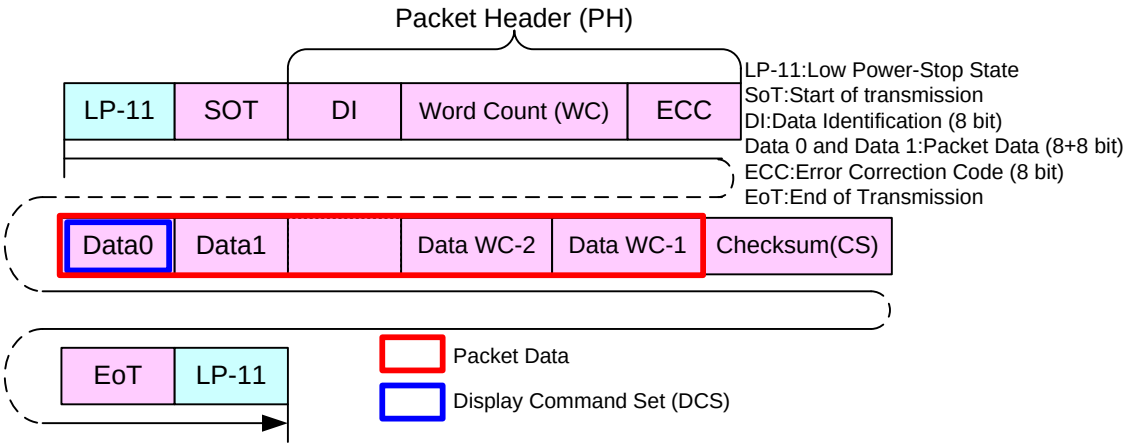


Figure 61 Display Command Set (DCS) on Short Packet (SPa) and Long Packet (LPa)

Generic Write, 1 Parameter (GENW1-S), Data Type = 01 0011 (13h)

"Generic Write, 1 Parameter" (GENW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0011b), from the MCU to the display module. The content of 2 payload bytes is "command" and 00h.

These commands are defined on a table (See chapter "9 Instruction Description") below

Command
NOP (00h)
SWRESET (01h)
SLPIN (10H)
SLPOUT (11h)
PTLON (12h)
NORON (13h)
INVOFF (20h)
INVON (21h)
ALLPOFF (22h)
ALLPON (23h)
DISPOFF (28h)
DISPON (29h)
IDMOFF (38h)
IDMON (39h)

Short Packet (SPa) is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 01 0011b

• Packet Data (PD)

  • Data 0: "Sleep In (10h)", Display Command Set (DCS)

  • Data 1: Always 00hex

• Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

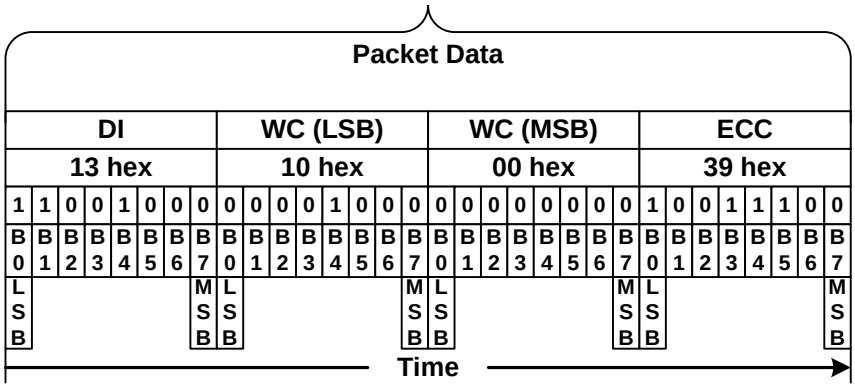


Figure 62 Generic Write,1 Parameter (GENW1-S)-Example

Generic Write, 2 Parameter (GENW2-S), Data Type = 10 0011 (23h)

"Generic Write, 2 Parameter" (GENW2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0011b), from the MCU to the display module. The content of 2 payload bytes is "command" and "parameter". These commands are defined on a table (See chapter "6 Instruction Description") below.

Command
GAMSET (26h)
COLMOD (3Ah)
WRDISBV (51h)
WRCTRLD (53h)
WRCABC (55h)
WRCABCMB (5Eh)

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 10 0011b
- Packet Data (PD)
  - Data 0: "PMCSET (3Ah)", Display Command Set (DCS)
  - Data 1: 01hex, Parameter of the DCS
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

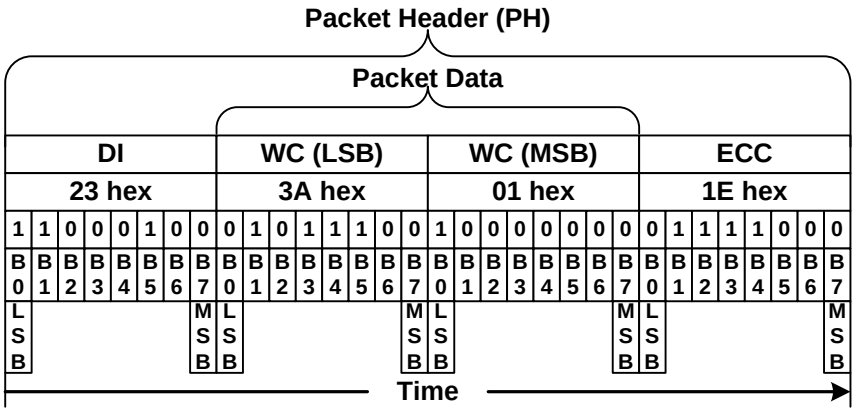


Figure 63 Generic Write, 2 Parameter (GENW2-S) – Example

Generic Write Long (GENW-L) , Data Type = 10 1001 (29h)

"Generic Write Long" (GENW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 10 1001b), from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters), are defined on a table (See chapter "6 Instruction Description") below.

Command		
NOP (00h) , Note1	INVON (21h) , Note1	IDMOFF (38h) , Note1
SWRESET (01h) , Note1	ALLPOFF (22h)	IDMON (39h) , Note1
SLPIN (10H) , Note1	ALLPON (23h)	COLMOD (3Ah) , Note2
SLPOUT (11h) , Note1	GAMSET (26h), , Note2	WRDISBV (51h) , Note2
PTLON (12h) , Note1	DISPOFF (28h) , Note1	WRCTRLD (53h) , Note2
NORON (13h) , Note1	DISPON (29h) , Note1	WRCABC (55h) , Note2
INVOFF (20h) , Note1	PARLINES (C5h)	WRCABCMB (5E) , Note2

Notes : 1. Also Short Packet (SPa) can be used; See Generic Write, 1 Parameter.
2. Also Short Packet (SPa) can be used; See Generic Write, 2 Parameter.c

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 10 1001b
- Word Count (WC)
  - Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: "Sleep In (10h)", Display Command Set (DCS)
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

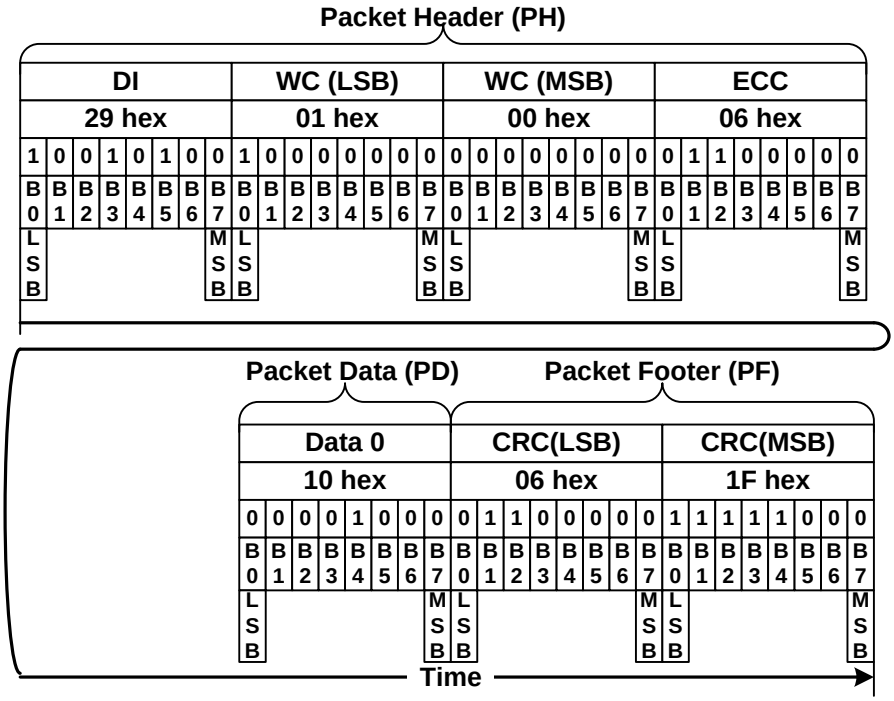


Figure 64 Generic Long Write(GENW-L) with DCS Only – Example

Long Packet (LPa), when a Write (1 parameter) was sent, is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 10 1001b

• Word Count (WC)

  • Word Count (WC): 0002h

• Error Correction Code (ECC)

• Packet Data (PD):

  • Data 0: “Gamma Set (3Ah)”, Display Command Set (DCS)

  • Data 1: 01hex, Parameter of the DCS

• Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

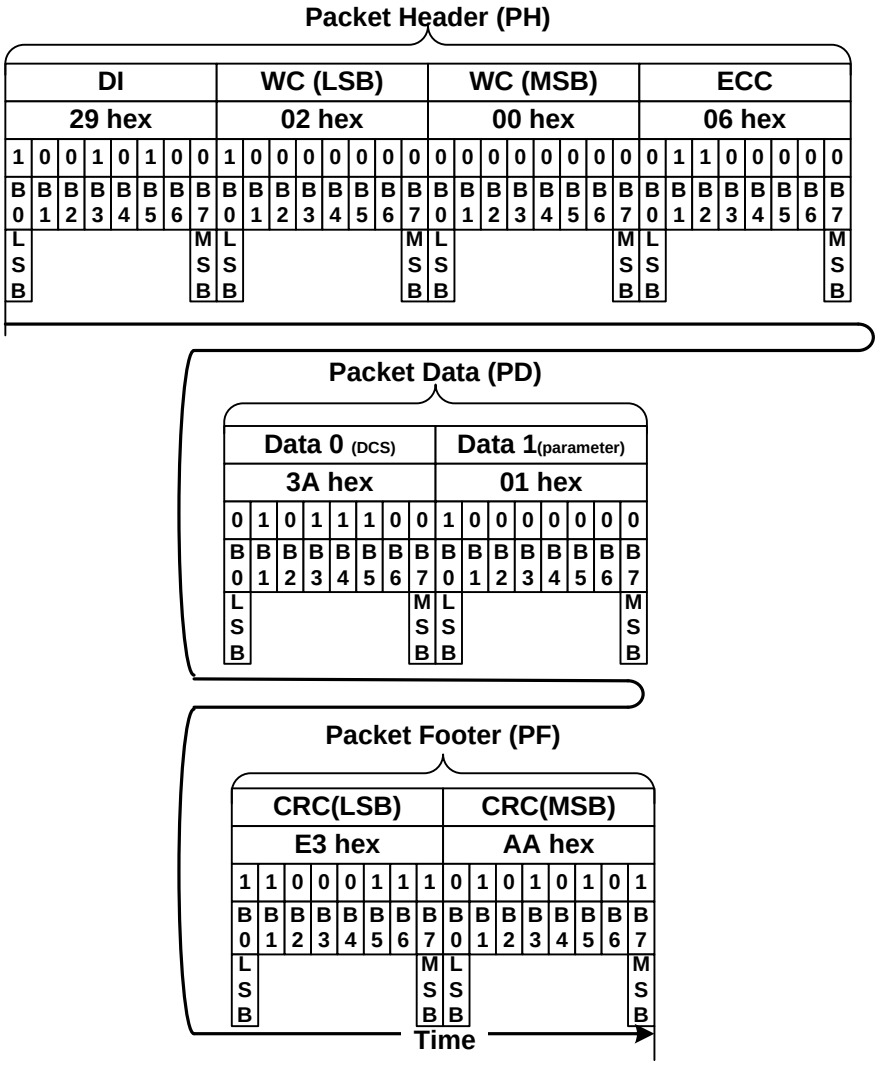


Figure 65 Generic Long Write (GENW-L) with DCS and 1 Parameter-Example

Long Packet (Lpa), when a Write (4 parameters) was sent, is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 10 1001b

• Word Count (WC)

  • Word Count (WC): 0005h

• Error Correction Code (ECC)

• Packet Data (PD):

  • Data 0: “PARLINES (30h)”, Display Command Set (DCS)

  • Data 1: 00hex, 1st Parameter of the DCS, Start Column SC[15…8]

  • Data 2: 00hex, 2nd Parameter of the DCS, Start Column SC[7…0]

  • Data 3: 01hex, 3rd Parameter of the DCS, End Column EC[15…8]

  • Data 4: 3Fhex, 4th Parameter of the DCS, End Column EC[7…0]

• Packet Footer (PF)

This is defined on the Long Packet (Lpa) as follows.

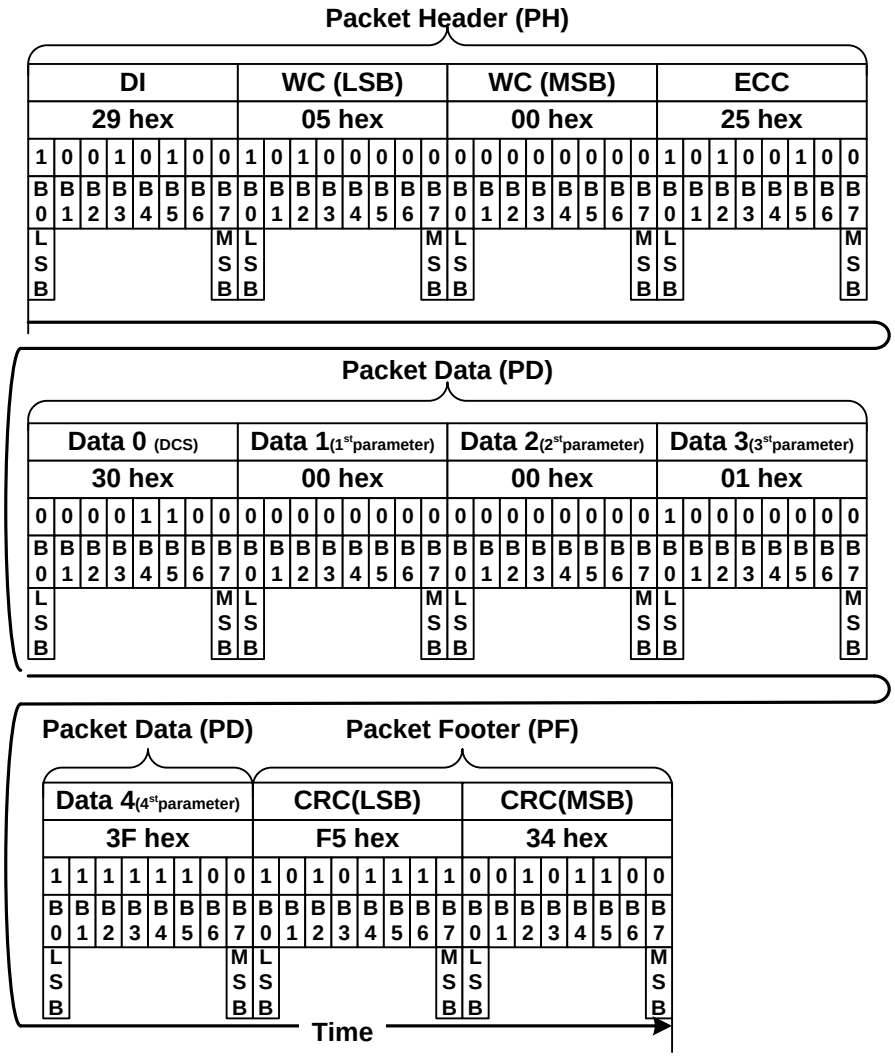


Figure 66 Generic Write Long (GENW-L) with DCS and 4 Parameters-Example

Generic Read, 1 Parameter (GENR1-S) , Data Type = 01 0100 (14h)

"Generic Read, 1 Parameter (GENR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT,01 0100b), from the MCU to the display module. This command is defined on a table (See chapter "9 Instruction Description") below.

Command	
RDDID (04h)	RDDSM (0Eh)
RDNUMED (05h)	RDDSDR (0Fh)
RDRED (06h)	RDDISBV (52h)
RDGREEN (07h)	RDCTRLD (54h)
RDBLUE (08h)	RDCABC (56h)
RDDPM (0Ah)	RDCABCMB (5Fh)
RDDMADCTR (0Bh)	RDID1 (DAh)
RDDCOLMOD (0Ch)	RDID2 (DBh)
RDDIM (0Dh)	RDID3 (DCh)

The MCU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send "Display Command Set (DCS) Read, No Parameter" to the display module. This same sequence is illustrated for reference purposes below.

Step 1:

• The MCU sends "Set Maximum Return Packet Size" (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 11 0111b

• Maximum Return Packet Size (MRPS)

  • Data 0: 01hex

  • Data 1: 00hex

• Error Correction Code (ECC)

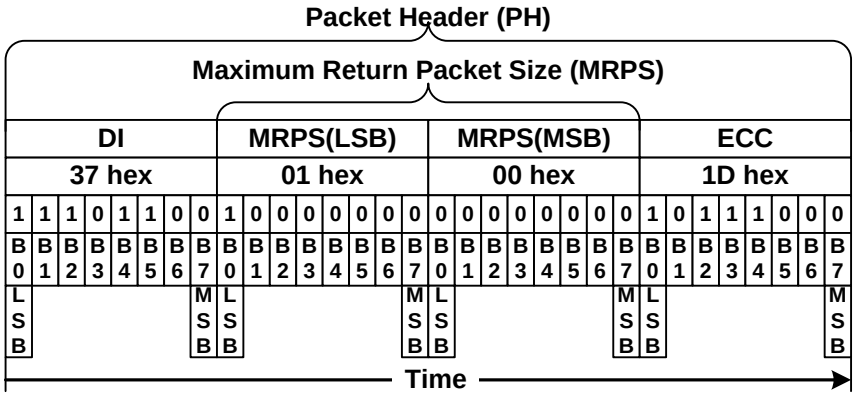


Figure 67 Set Maximum Return Packet Size (SMRPS-S)- Example

Step 2:

• The MCU wants to receive a value of the “Read ID1 (DAh)” from the display module when the MCU sends “Generic Read, 1 Parameter” to the display module

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 01 0100b

• Packet Data (PD)

  • Data 0: “Read ID1 (DAh)”, Display Command Set (DCS)

  • Data 1: Always 00hex

• Error Correction Code (ECC)

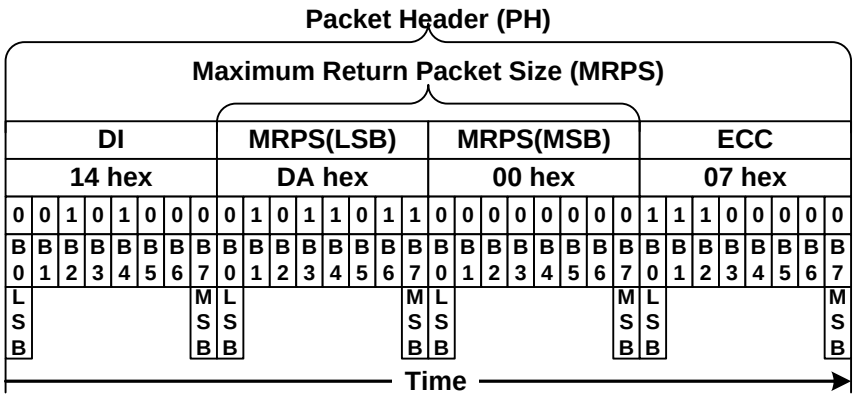


Figure 68 Generic Read, 1 Parameter (GENR1-S) – Example

Step 3: The display module can send 2 different information to the MCU after Bus Turnaround (BTA)

1. An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command. See section “Acknowledge with Error Report (AwER)”.

2. Information of the received command. Short Packet (SPa) or Long Packet (LPa)

Display Command Set (DCS) Write, No Parameter (DCSWN-S) , Data Type = 00 0101 (05h)

"Display Command Set (DCS) Write, No Parameter" is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0101b), from the MCU to the display module. These commands are defined on a table (See chapter "9 Instruction Description") below.

Command	
NOP (00h)	INVON (21h)
SWRESET (01h)	ALLPOFF (22h)
SLPIN (10h)	ALLPON (23h)
SLPOUT (11h)	DISPOFF (28h)
PTLON (12h)	DISPON (29h)
NORON (13h)	IDMOFF (38h)
INVOFF (20h)	IDMON (39h)

Short Packet (SPa) is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 00 0101b

• Packet Data (PD)

  • Data 0: "Sleep In (10h)", Display Command Set (DCS)

  • Data 1: Always 00hex

• Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

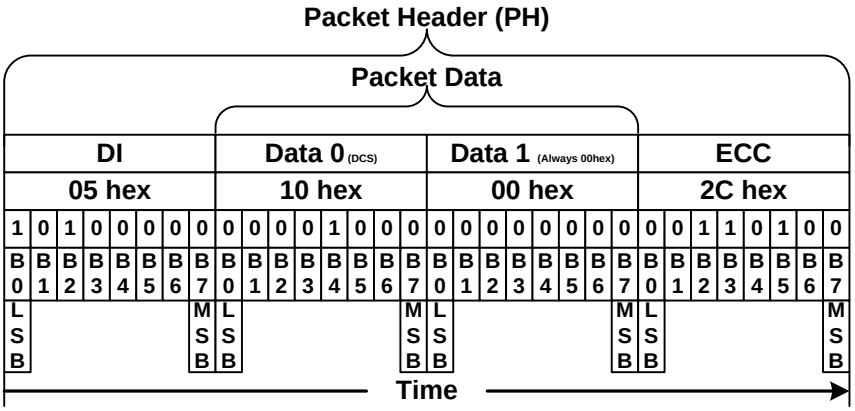


Figure 69 Display Command Set (DCS) Write,No Parameter(DCSWN-S)-Example

Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) , Data Type = 01 0101 (15h)

"Display Command Set (DCS) Write, 1 Parameter" (DCSW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0101b), from the MCU to the display module. These commands are defined on a table (See chapter "9 Instruction Description") below.

Command
GAMSET (26h)
COLMOD (3Ah)
WRDISBV (51h)
WRCTRLD (53h)
WRCABC (55h)
WRCABCMB (5Eh)

Short Packet (SPa) is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 01 0101b

• Packet Data (PD)

  • Data 0: "PMCSET (3Ah)", Display Command Set (DCS)

  • Data 1: 01hex, Parameter of the DCS

• Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

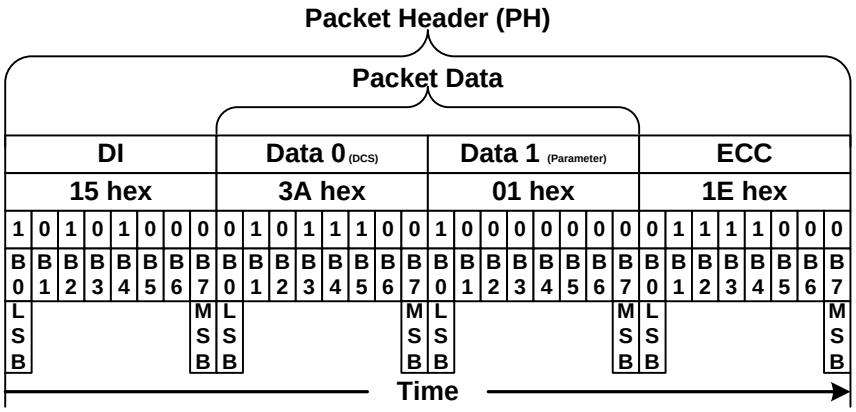


Figure 70 Display Command Set (DCS) Write,1 Parameter (DCSW1-S)-Example

Display Command Set (DCS) Write Long (DCSW-L) , Data Type = 11 1001 (39h)

"Display Command Set (DCS) Write Long" (DCSW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 11 1001b), from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters), are defined on a table (See chapter "9 Instruction Description") below

Command		
NOP (00h) , Note1	INVON (21h) , Note1	COLMOD (3Ah) , Note2
SWRESET (01h) , Note1	GAMSET (26h) , Note2	WRDISBV (51h), Note2
SLPIN (10h) , Note1	DISPOFF (28h) , Note1	WRCTRLD (53h)
SLPOUT (11h) , Note1	DISPON (29h), Note1	WRCABC (55h) , Note2
PTLON (12h) , Note1	PARLINES (30h)	WRCABCMB (5Eh)
NORON (13h), Note1	IDMOFF (38h) , Note1	
INVOFF (20h), Note1	IDMON (39h) , Note1	

Notes：1. Also Short Packet (SPa) can be used; See_Display Command Set (DCS) Write, No Parameter.
2. Also Short Packet (SPa) can be used; See Display Command Set (DCS) Write, 1 Parameter.

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 11 1001b

• Word Count (WC)

  • Word Count (WC): 0001h

• Error Correction Code (ECC)

• Packet Data (PD): Data 0: "Sleep In (10h)", Display Command Set (DCS)

• Packet Footer (PF)

This is defined on the Short Packet (SPa) as follows.

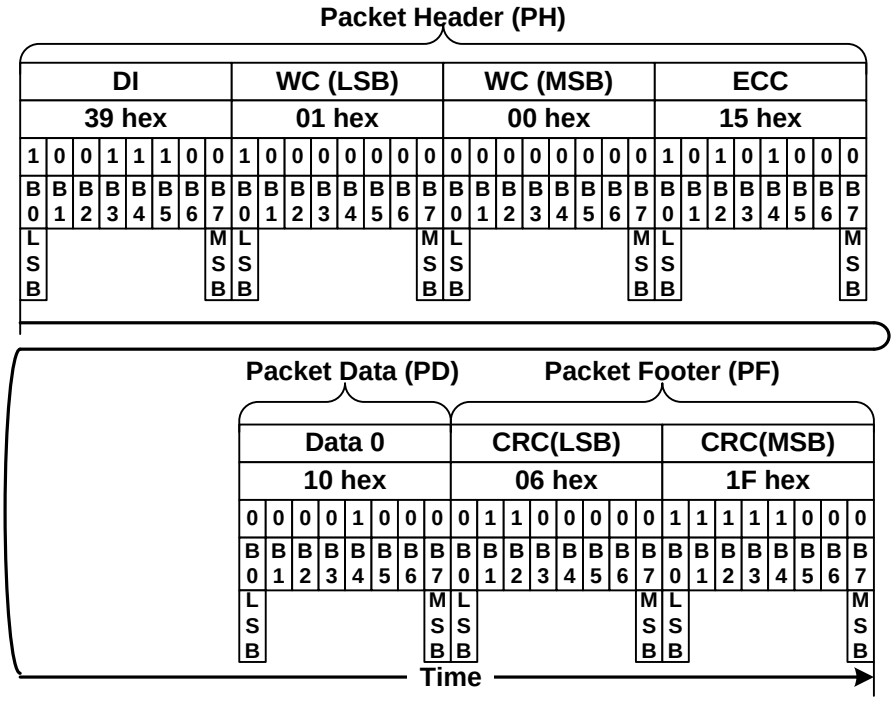


Figure 71 Display Command Set (DCS) Write Long (DCSW-L) with DCS Only-Example

Long Packet (LPa), when a Write (1 parameter) was sent, is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 11 1001b

• Word Count (WC)

  • Word Count (WC): 0002h

• Error Correction Code (ECC)

• Packet Data (PD):

  • Data 0: “Gamma Set (26h)”, Display Command Set (DCS)

  • Data 1: 01hex, Parameter of the DCS

• Packet Footer (PF)

This is defined on the Short Packet (SPa) as follows

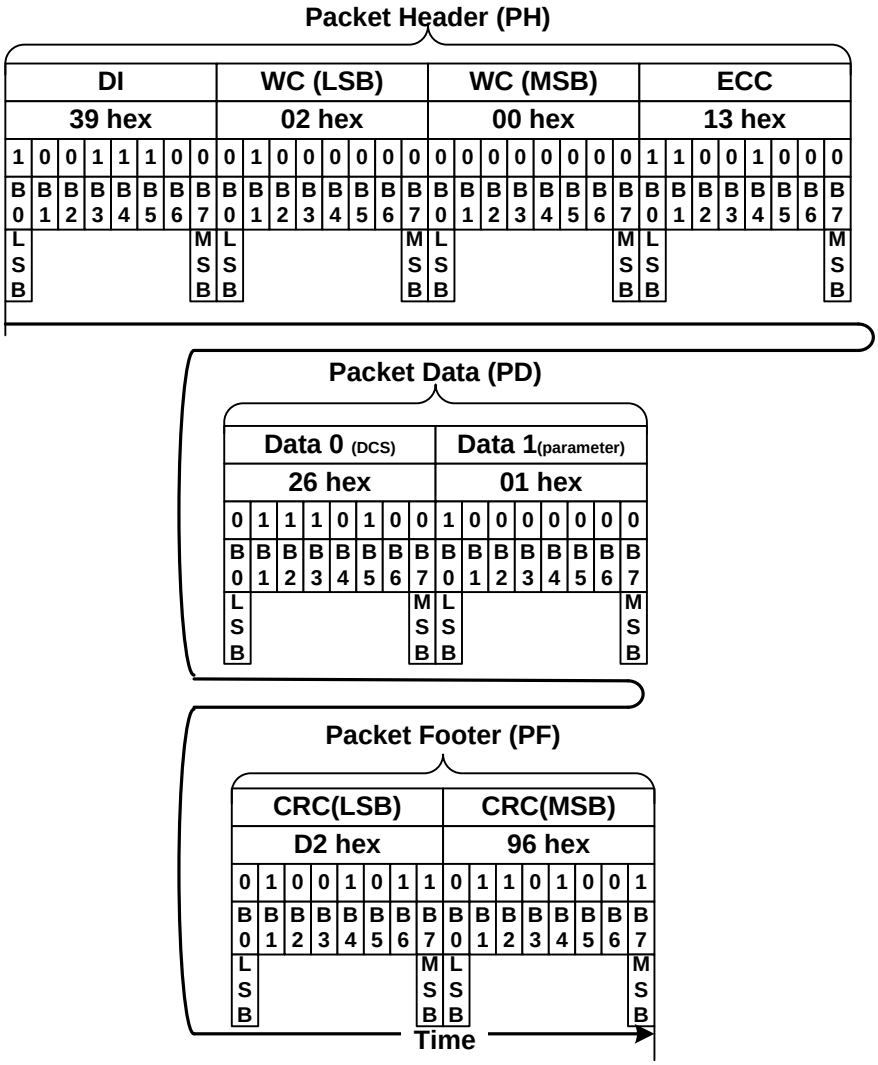


Figure 72 Display Command Set (DCS) Write Long with DCS and 1 Parameter-Example

Long Packet (LPa), when a Write (4 parameters) was sent, is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 11 1001b

• Word Count (WC)

  • Word Count (WC): 0005h

• Error Correction Code (ECC)

• Packet Data (PD):

  • Data 0: “PARLINES (30h)”, Display Command Set (DCS)

  • Data 1: 00hex, 1st Parameter of the DCS, Start Column SC[15…8]

  • Data 2: 00hex, 2nd Parameter of the DCS, Start Column SC[7…0]

  • Data 3: 01hex, 3rd Parameter of the DCS, End Column EC[15…8]

  • Data 4: 3Fhex, 4th Parameter of the DCS, End Column EC[7…0]

• Packet Footer (PF)

This is defined on the Short Packet (SPa) as follows.

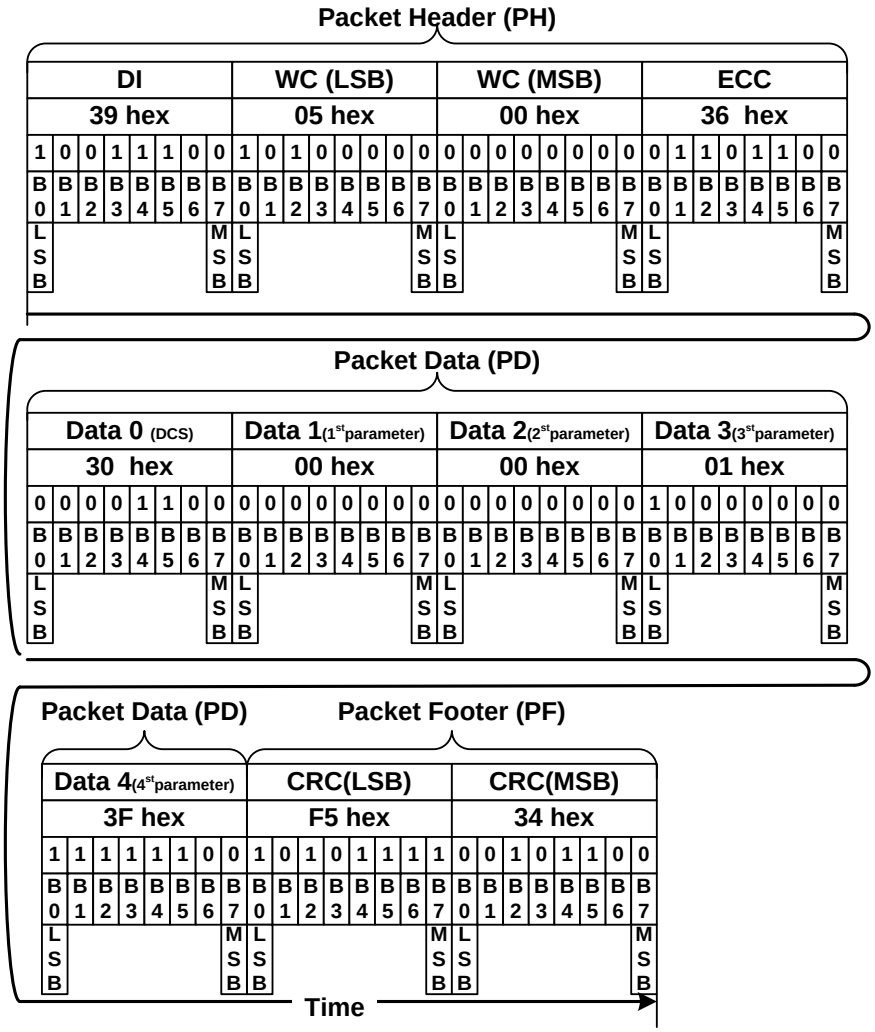


Figure 73 Display Command Set (DCS) Write Long with DCS and 4 Parameters-Example

Display Command Set (DCS) Read, No Parameter (DCSRN-S), Data Type = 00 0110 (06h)

"Display Command Set (DCS) Read, No Parameter" (DCSRN-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0110b), from the MCU to the display module. These commands are defined on a table (See chapter "9 Instruction Description") below.

Command	
RDDID (04h)	RDDSM (0Eh)
RDNUMED (05h)	RDDSDR (0Fh)
RDRED (06h)	RDDISBV (52h)
RDGREEN (07h)	RDCTRLD (54h)
RDBLUE (08h)	RDCABC (56h)
RDDPM (0Ah)	RDCABCMB (5Fh)
RDDMADCTR (0Bh)	RDID1 (DAh)
RDDCOLMOD (0Ch)	RDID2 (DBh)
RDDIM (0Dh)	RDID3 (DCh)

The MCU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send "Display Command Set (DCS) Read, No Parameter" to the display module. This same sequence is illustrated for reference purposes below.

Step 1:

• The MCU sends "Set Maximum Return Packet Size" (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 11 0111b

• Maximum Return Packet Size (MRPS)

  • Data 0: 01hex

  • Data 1: 00hex

• Error Correction Code (ECC)

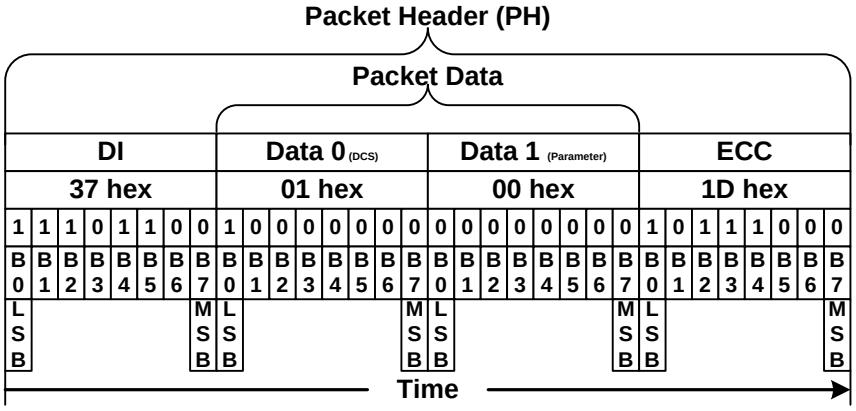


Figure 74 Set Maximum Return Packet Size (SMRPS-S) - Example

Step 2:

• The MCU wants to receive a value of the “Read ID1 (DAh)” from the display module when the MCU sends “Display Command Set (DCS) Read, No Parameter” to the display module

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 00 0110b

• Packet Data (PD)

  • Data 0: “Read ID1 (DAh)”, Display Command Set (DCS)

  • Data 1: Always 00hex

• Error Correction Code (ECC)

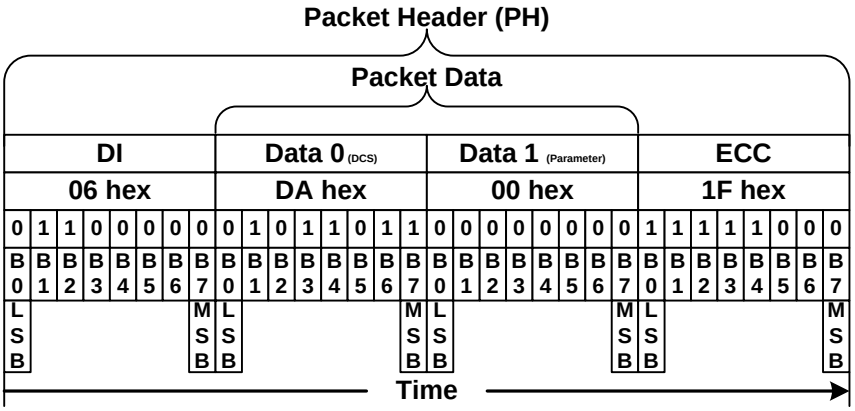


Figure 75 Display Command Set (DCS) Read, No Parameter (DCSRN-S) – Example

Step 3: The display module can send 2 different information to the MCU after Bus Turnaround (BTA)

1. An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command. See section “Acknowledge with Error Report (AwER)”.

2. Information of the received command. Short Packet (SPa) or Long Packet (LPa)

Null Packet, No Data (NP-L) , Data Type = 00 1001 (09h)

"Null Packet, No Data" (NP-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 001001b),from the MCU to the display module. The purpose of this command is keeping data lanes in the high speed mode (HSDT), if it is needed. The display module is ignored Packet Data (PD) what the MCU is sending.

Long Packet (LPa), when 5 random data bytes of the Packet Data (PD) were sent, is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 00 1001b

• Word Count (WC)

  • Word Count (WC): 0005h

• Error Correction Code (ECC)

• Packet Data (PD):

  • Data 0: 89h (Random data)

  • Data 1: 23h (Random data)

  • Data 2: 12h (Random data)

  • Data 3: A2h (Random data)

  • Data 4: E2h (Random data)

• Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

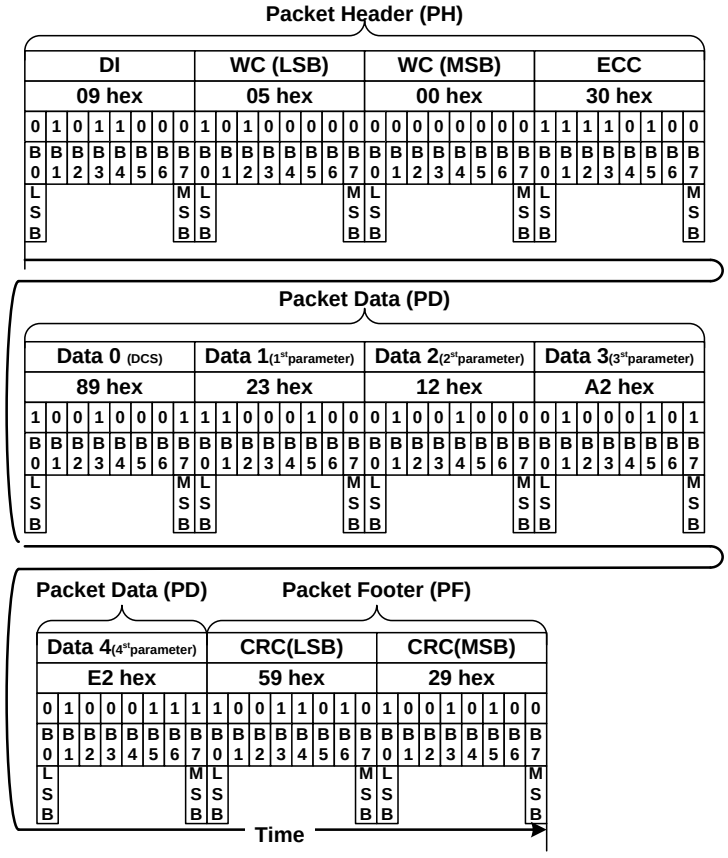


Figure 76 Null Packet, No Data (NP-L)-Example

End of Transmission Packet (EoTP), Data Type = 00 1000 (08h)

"End of Transmission Packet" (EoTP) is always using a Short Packet (SPa), what is defined on Data Type (DT, 001000b), from the MCU to the display module. The purpose of this command is terminated the high speed mode (HPDT) properly when there is added this extra packet after the last payload packet before "End of Transmission" (EoT), which is an interface level functionality.

The MCU can decide if it want to use the "End of Transmission Packet" (EoTP) or not. The ST7701S has the capability to support both: i.e. If MCU applies the EoTP, it shall report the "DSI Protocol Violation" error when the EoTP is not detected in the high speed (HS). This error reporting can be enable/disable by bit DIS_EoTP_HS of command B100h (page 0).

The display module is or isn't receiving "End of Transmission Packet" (EoTP) from the MCU during the Low Power Data Transmission (LPDT) mode before "Marked-1" (=leaving Escape mode) what ends the Low Power Data Transmission (LPDT) mode.

The display module is not allowed to send "End of Transmission Packet" (EoTP) to MCU during the Low Power Data Transmission (LPDT) mode.

The summary of the receiving and transmitting EoTP is listed below.

Direction	Display Module (DM) in High Speed Data Transmission (HPDT)	Display Module (DM) in Low Power Data Transmission (LPDT)
MCU=>Display Driver	With or Without EoTP is Supported	With or Without EoTP is Supported
Display Driver=>MCU	HS Mode is not available (EoTP is not available)	EoTP can not be sent by the Display Driver

Table 17 Receiving and Transmitting EoTP during LPDT

Short Packet (SPa) is using a fixed format as follow

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 00 1000b

• Packet Data (PD):

  • Data 0: 0Fh

  • Data 1: 0Fh

• Error Correction Code (ECC)

• ECC: 01h

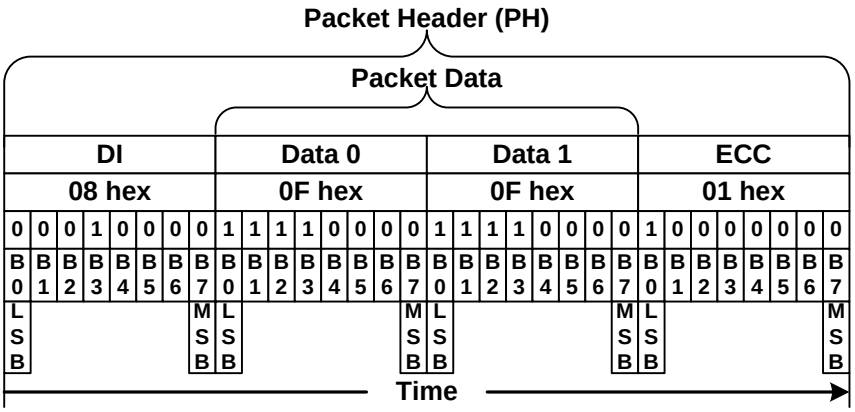


Figure 77 End of Transmission Packet (EoTP)

Some use case of the “End of Transmission Packet” (EoTP) are illustrated only for reference purpose below.

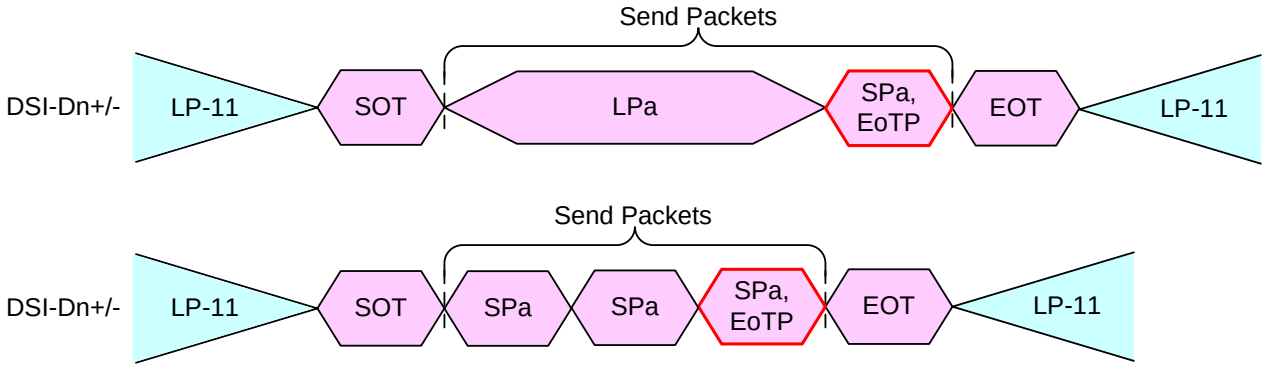


Figure 78 End of Transmission Packet (EoTP)-Example

Sync Event (H Start, H End, V Start, V End), Data Type = xx 0001 (x1h)

Sync Events are Short packets and, therefore, can time-accurately represent events like the start and end of sync pulses. As “start” and “end” are separate and distinct events, the length of sync pulses, as well as position relative to active pixel data, e.g. front and back porch display timing, may be accurately conveyed to the peripheral. The Sync Events are defined as follows:

- Data Type = 00 0001 (01h) V Sync Start
- Data Type = 01 0001 (11h) V Sync End
- Data Type = 10 0001 (21h) H Sync Start
- Data Type = 11 0001 (31h) H Sync End

In order to represent timing information as accurately as possible a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Similarly, a V Sync End event implies an H Sync Start event for the last line of the VSA..

Sync events should occur in pairs, Sync Start and Sync End, if accurate 1054 pulse-length information needs to be conveyed. Alternatively, if only a single point (event) in time is required, a single sync event (normally, Sync Start) may be transmitted to the peripheral. Sync events may be concatenated with blanking packets to convey inter-line timing accurately and avoid the overhead of switching between LPS and HS for every event. Note there is a power penalty for keeping the data line in HS mode, however. Display modules that do not need traditional sync/blanking/pixel timing should transmit pixel data in a high-speed burst then put the bus in Low Power Mode, for reduced power consumption. The recommended burst size is a scan line of pixels, which may be temporarily stored in a line buffer on the display module.

Color Mode On Command, and, Data Type = 01 0010 (12h)

Color Mode On is a Short packet command that switches a Video Mode display module to 8-colors mode for power saving.

Color Mode Off Command, Data Type = 00 0010 (02h)

Color Mode Off is a Short packet command that returns a Video Mode display module from 8-colors mode to normal display operation.

Shutdown Peripheral Command, Data Type = 10 0010 (22h)

Shutdown Peripheral command is a Short packet command that turns off the display in a Video Mode display module for power saving. Note the interface shall remain powered in order to receive the turn-on, or wake-up, command.

Turn On Peripheral Command, Data Type = 11 0010 (32h)

Turn On Peripheral command is Short packet command that turns on the display in a Video Mode display module for normal display operation.

Blanking Packet (Long), Data Type = 01 1001 (19h)

A Blanking packet is used to convey blanking timing information in a Long packet. Normally, the packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the display module. The blanking period may have Sync Event packets interspersed between blanking segments. Like all packets, the Blanking packet contents shall be an integer number of bytes. Blanking packets may contain arbitrary data as payload. The Blanking packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes, and a two-byte checksum.

Packed Pixel Stream, 16-bit Format, Long packet, Data Type = 00 1110 (0Eh)

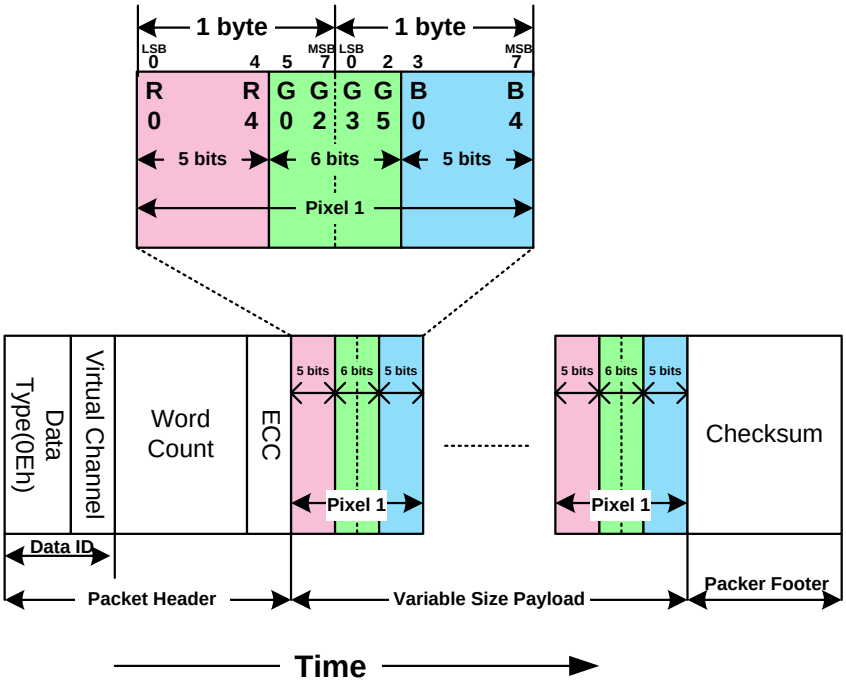


Figure 79 16-bit per Pixel-RGB Color Format, Long packet

Packed Pixel Stream 16-Bit Format is a Long packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is five bits red, six bits green, five bits blue, in that order. Note that the “Green” component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every two bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

Normally, the display module has no frame buffer of its own, so all image data shall be supplied by the host processor at a sufficiently high rate to avoid flicker or other visible artifacts.

Packed Pixel Stream, 18-bit Format, Long packet, Data type = 01 1110 (1Eh)

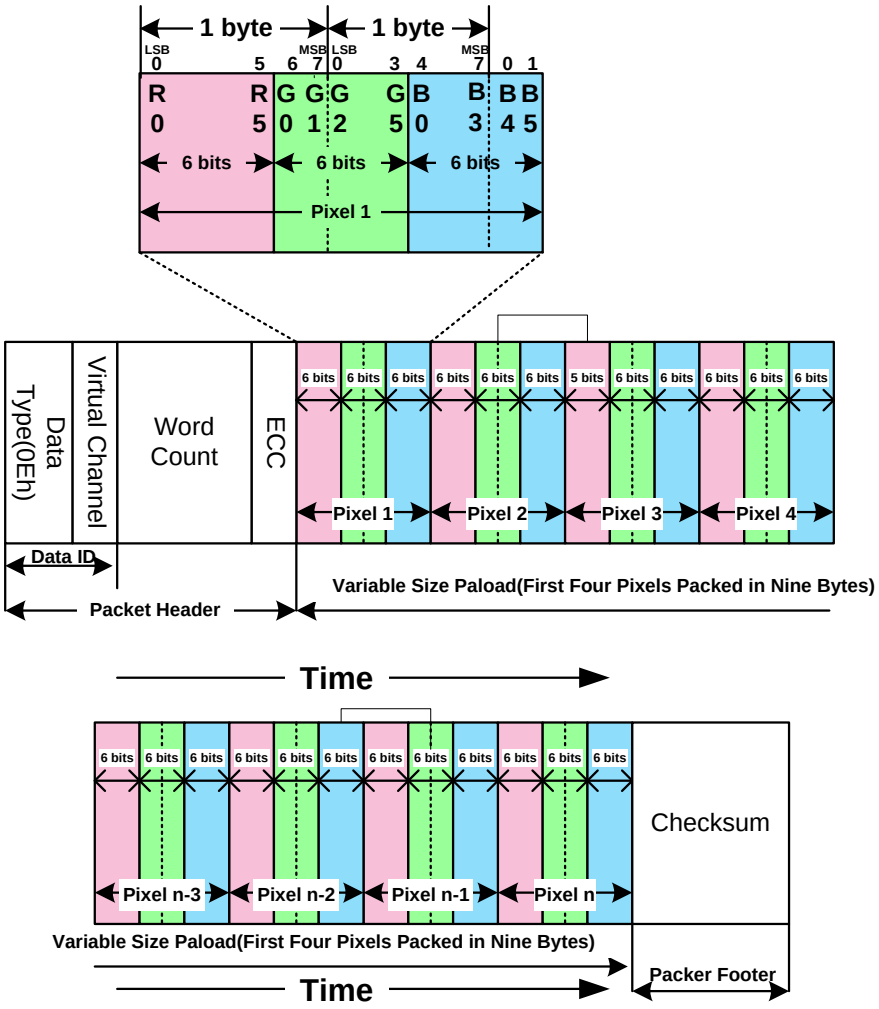


Figure 80 18-bit per Pixel-RGB Color Format, Long pack

Packed Pixel Stream 18-Bit Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. The receiving peripheral shall not display the fill pixels when refreshing the display device. For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the transmission.

With this format, the total line width (displayed plus non-displayed pixels) should be a multiple of four pixels (nine bytes).

Pixel Stream, 18-bit Format in Three Bytes, Long packet, Data Type = 101110 (2Eh)

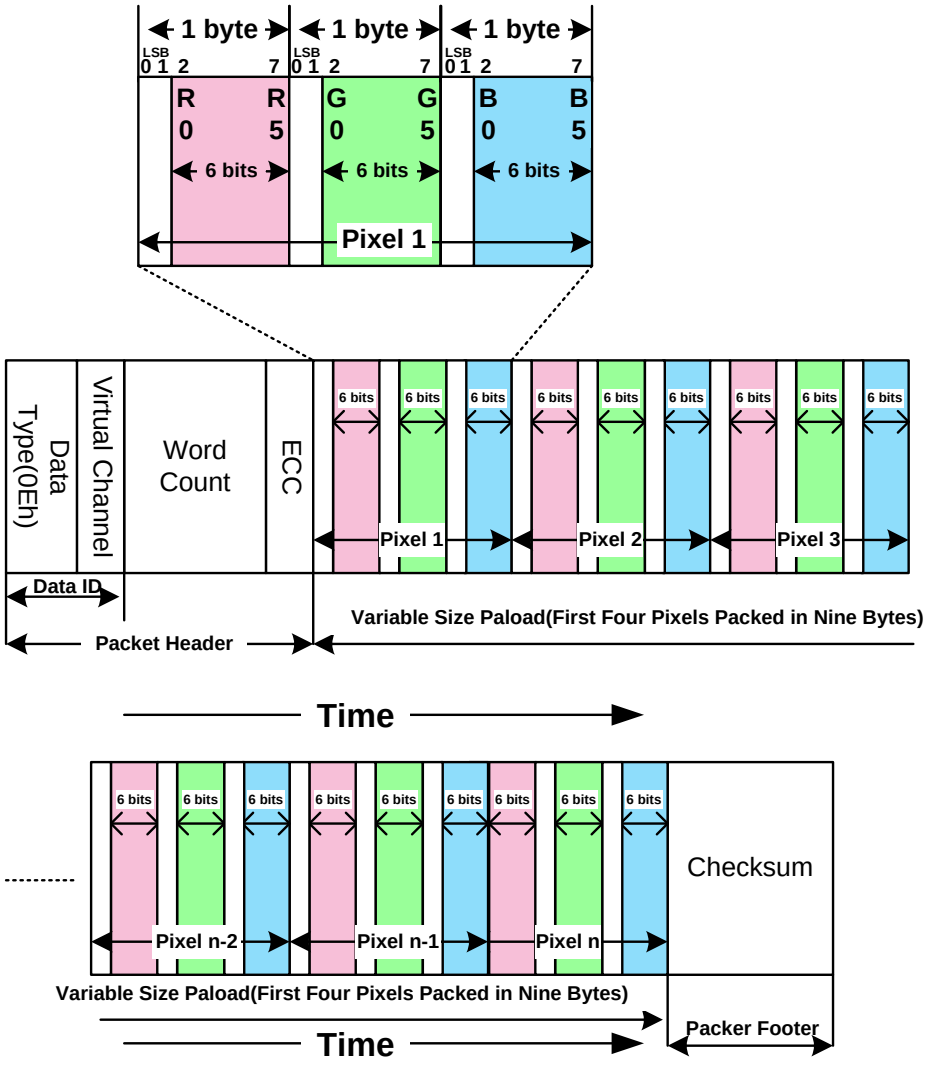


Figure 81 18-bit per Pixel (Loosely Packed)-RGB Color Format, Long pack

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the Link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

Packed Pixel Stream, 24-bit Format, Long packet, Data Type = 11 1110 (3Eh)

Packed Pixel Stream 24-Bit Format is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

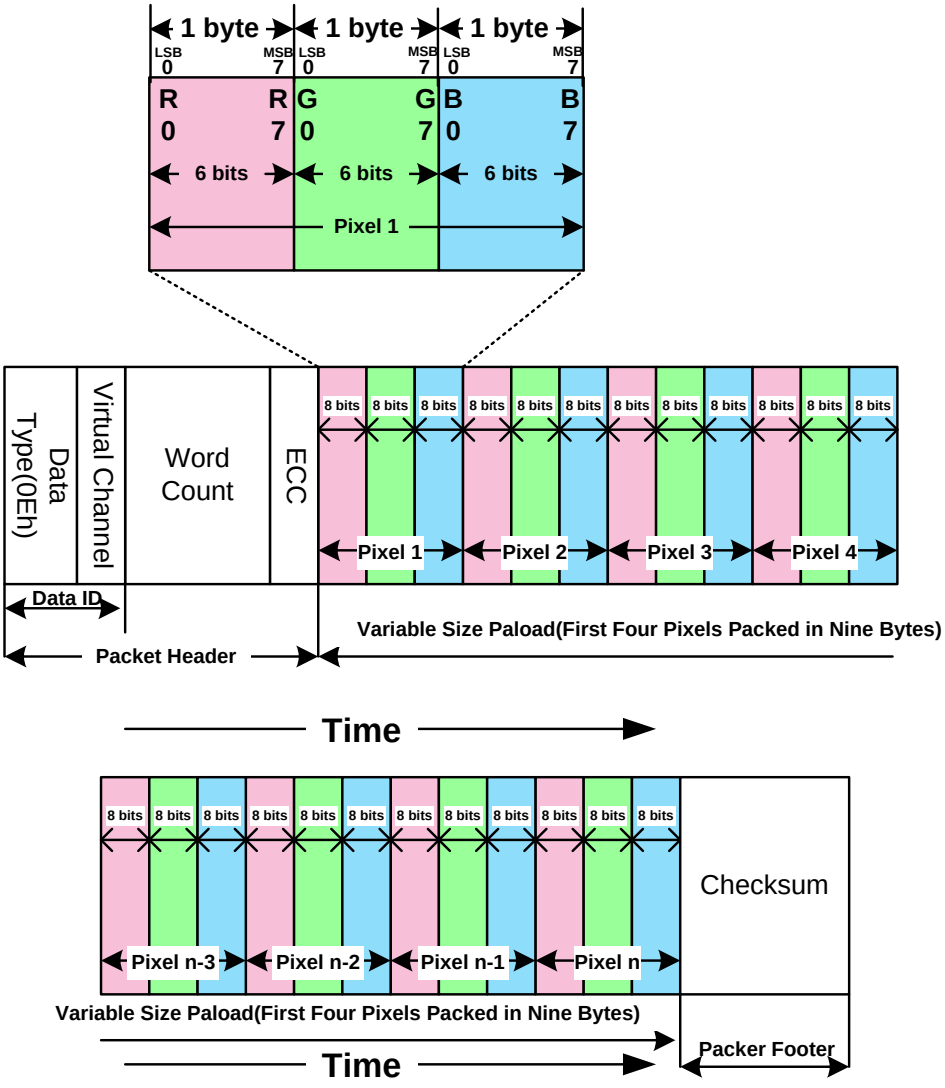


Figure 82 24-bit per Pixel -RGB Color Format, Long packet

8.7.2.3.2.2 PACKET FROM THE DISPLAY MODULE TO THE MCU

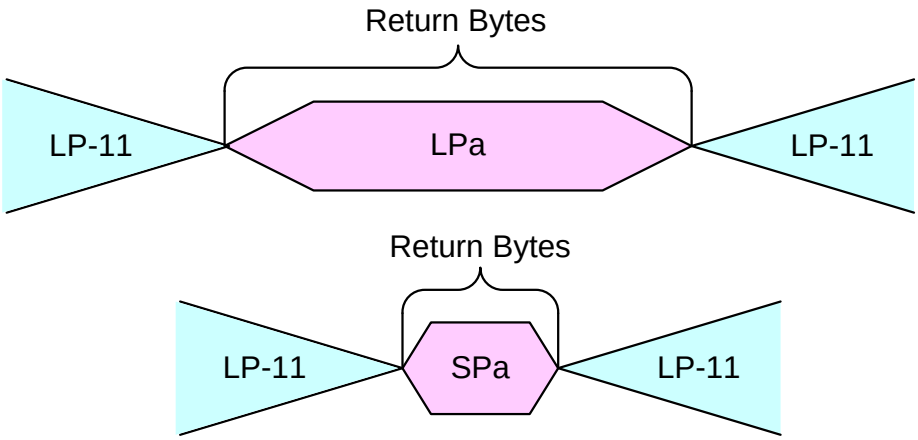
Used Packet Types

The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) Read, No Parameter",(DCSRN-S)) or an Acknowledge with Error Report .The used packet type is defined on Data Type (DT)..

A number of the return bytes are more than the maximum size of the Packet Data (PD) on Long Packet (LPa) or Short Packet (SPa) when the display module is sending return bytes in several packets until all return bytes have been sent from the display module to the MCU.

It is not possible that the display module is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent on a packet.

Both cases are illustrated for reference purposes below.

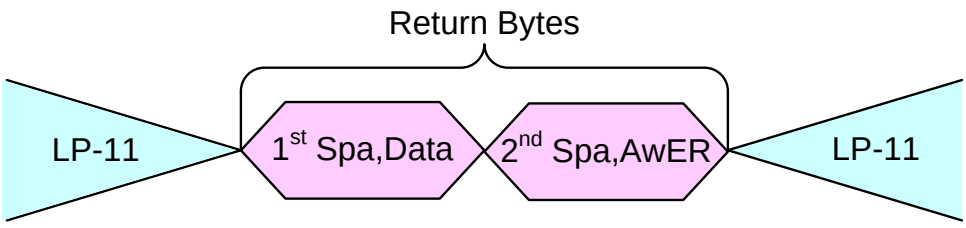


Return Bytes on Signal Packet

Data Type Hex	Data Type Binary	Symbol	Description	Packet Size
02h	00 0010	AwER	Acknowledge & Error Report	Short
1Ch	01 1100	DCSRR-L	DCS Long Read Response	Long
21h	10 0001	SCSRR1-S	DCS Short Read Response, 1 Byte returned	Short
22h	01 0010	DCSRR2-S	DCS Short Read Response, 2 Byte returned	Short
1Ah	01 1010	GENRR-L	Generic Long Read Response	Long
11h	01 0001	GENRR1-S	Generic Long Read Response, 1 Byte returned	Short
12h	01 0010	GENRR2-S	Generic Long Read Response, 2 Byte returned	Short

Table 18 Data Type for Display Module-sourced Packets

The display module is return 2 packets (1st packet: Data, 2nd packet Acknowledge with Error Report) to the MCU when the display module has received a read command. See section “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” where has been detected and corrected a single bit error by the EEC (See bit 8 on Table” Acknowledge with Error Report (AwER) for Short Packet (SPa) Response”). This return packets are illustrated for reference purpose below.



Exception When Return Bytes on Several Packet

AwER=Acknowledge with Error Report

Acknowledge with Error Report (AwER), Data Type = 00 0010(02h)

"Acknowledge with Error Report" (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT,00 0010b), from the display module to the MCU.

The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to '1',as they are defined on the following table.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to '0' internally
15	DSI Protocol Violation

Table 19 Acknowledge with Error Report (AwER) for Long Packet (LPa) Response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Set to "0" internally (Only for Long Packet (LP))
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to '0' internally
15	DSI Protocol Violation

Table 20 Acknowledge with Error Report (AwER) for Short Packet (SPa) Response

These errors are only included on the last packet, which has been received from the MCU to the display module before Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors

Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 00 0010b

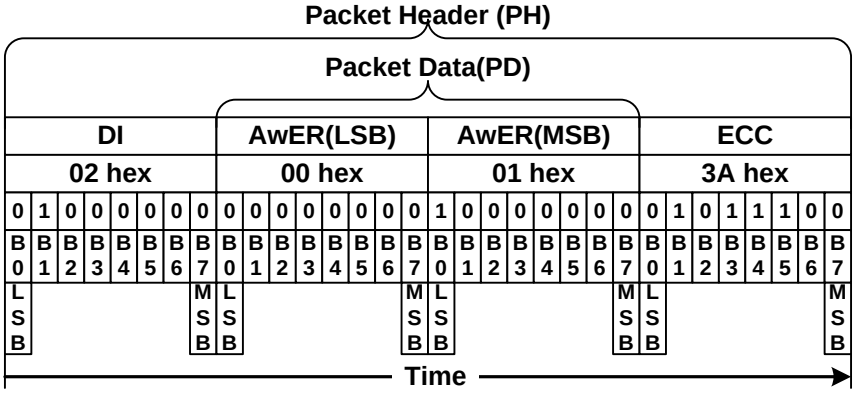
• Packet Data (PD):

  • Bit 8: ECC Error, single-bit (detected and corrected)

  • AwER: 0100h

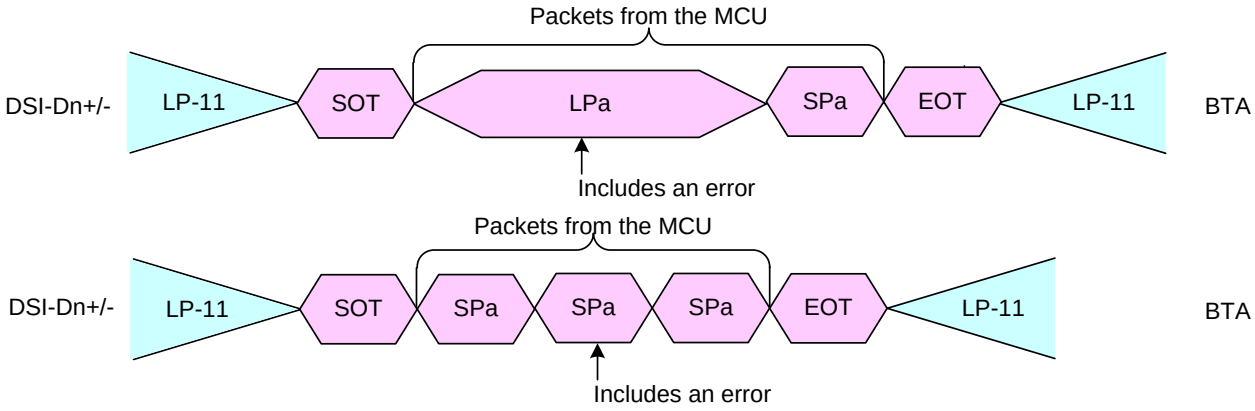
• Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Acknowledge with Error Report (AwER)-Example

It is possible that the display module receivers several packets, which include error, from the MPU before the MPU performs the Bus Turnaround (BTA).Some examples are illustrated below for reference purpose.



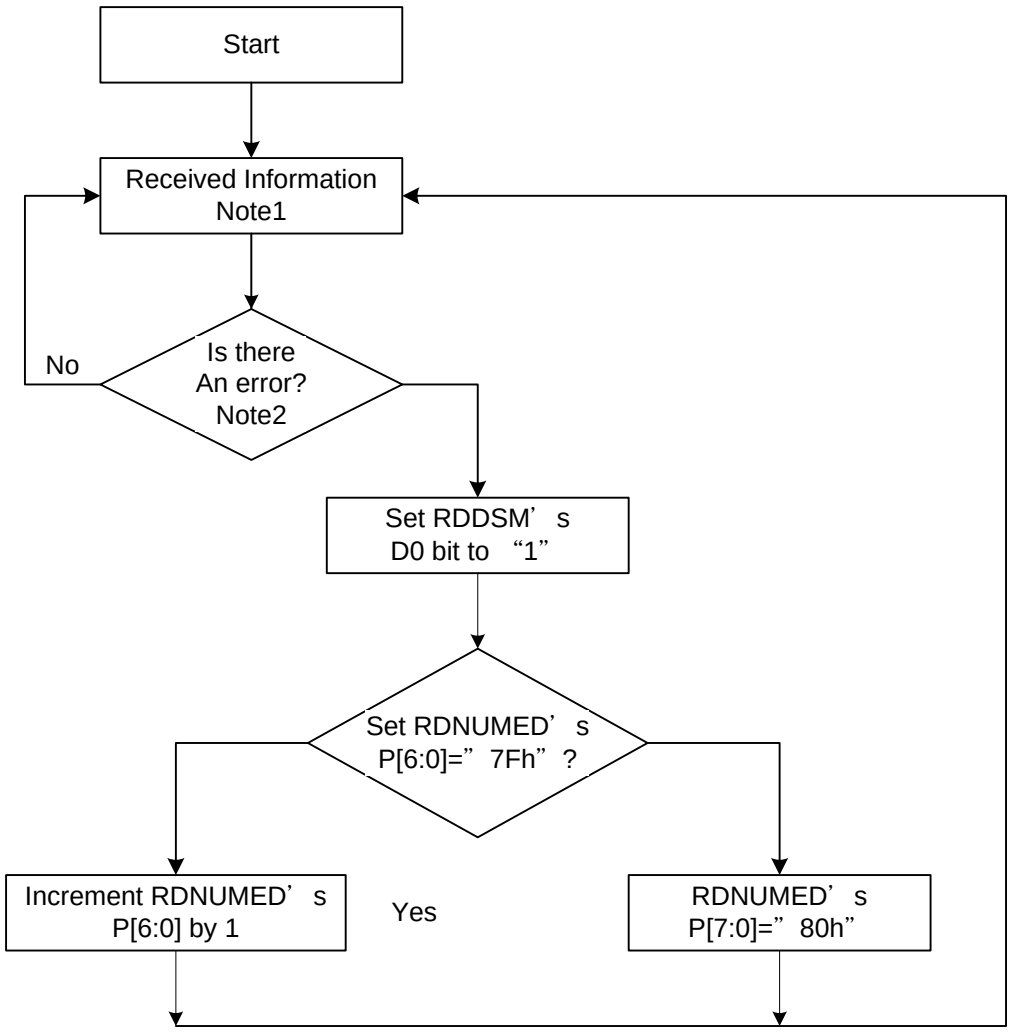
Error Packet

Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)”commands.

The bit D0 of the “Read Display Signal Mode (0Eh)” command has been set to ‘1’ if a received packet includes an error.

The number of the packets, which are including an ECC or CRC error, are calculated on the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h as well as set the bit D0 of the “Read Display Signal Mode (0Eh)” command to ‘0’ after the MCU has read the RDNUMED register from the display module.

The functionality of the RDNUMED register is illustrated for reference purposes below.



Notes:

1. This information can Interface or Packet Level Communication but it is always from the MCU to the display module in this case.

2. CRC or ECC error.

DCS Read Long Response (DCSRR-L), Data Type = 01 1100(1Ch)

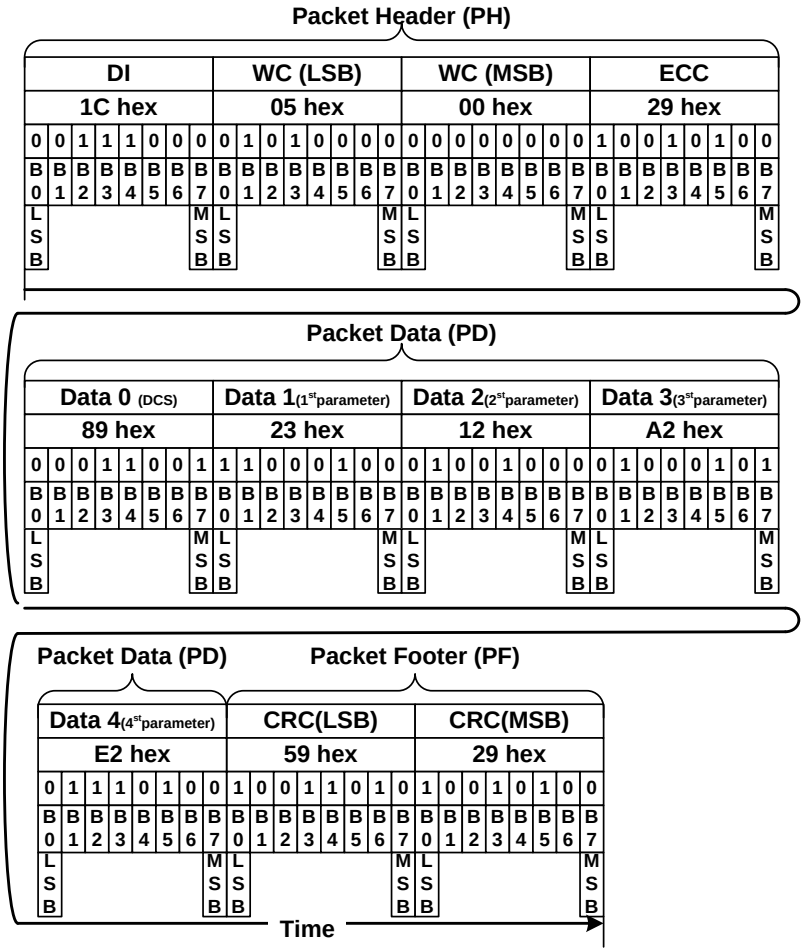
"DCS Read Long Response" (DCSRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT,01 1100b), from the display module to the MCU. "DCS Read Long Response" (DCSRR-L) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

"DCS Read Long Response" (DCSRR-L) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

- Data Identification (DI)
    - Virtual Channel (VC, DI[7…6]): 00b
    - Data Type (DT, DI[5…0]): 01 1100b
- Word Count (WC)
    - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
    - Data 0: 89h
    - Data 1: 23h
    - Data 2: 12h
    - Data 3: A2h
    - Data 4: E2h
- Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.



DCS Read Long Response(DCSRR-L)-Example

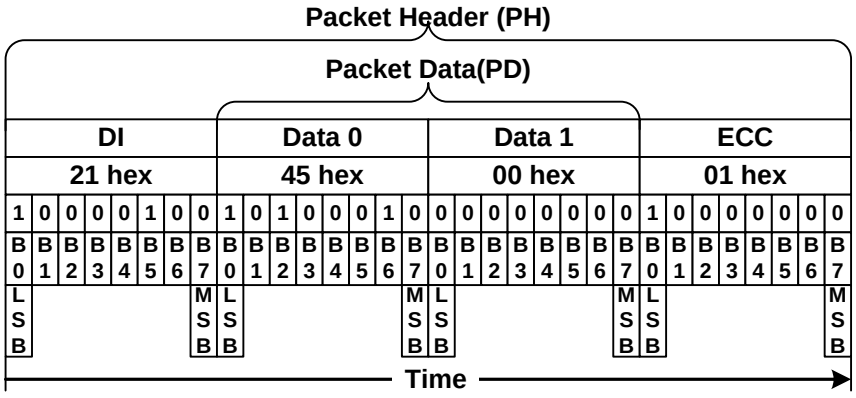
DCS Read Short Response, 1 Byte Returned (DCSRR1-S), Data Type = 10 0001(21h)

"DCS Read Short Response, 1 Byte Returned" (DCSRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0001b), from the display module to the MCU. "DCS Read Short Response, 1 Byte Returned" (DCSRR1-S) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

• Data Identification (DI)
  • Virtual Channel (VC, DI[7…6]): 00b
  • Data Type (DT, DI[5…0]): 10 0001b
• Packet Data (PD):
  • Data 0: 45h
  • Data 1: 00h (Always)
• Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.



DCS Read Short Response,1 Byte Returned(DCSRR1-S)-Example

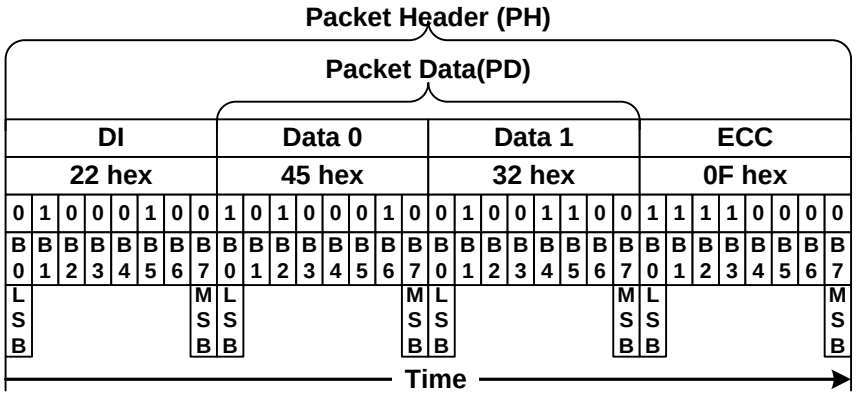
DCS Read Short Response, 2 Bytes Returned (DCSRR2-S), Data Type = 10 0010(22h)

"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0010b), from the display module to the MCU. "DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 10 0010b
- Packet Data (PD):
  - Data 0: 45h
  - Data 1: 32h
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



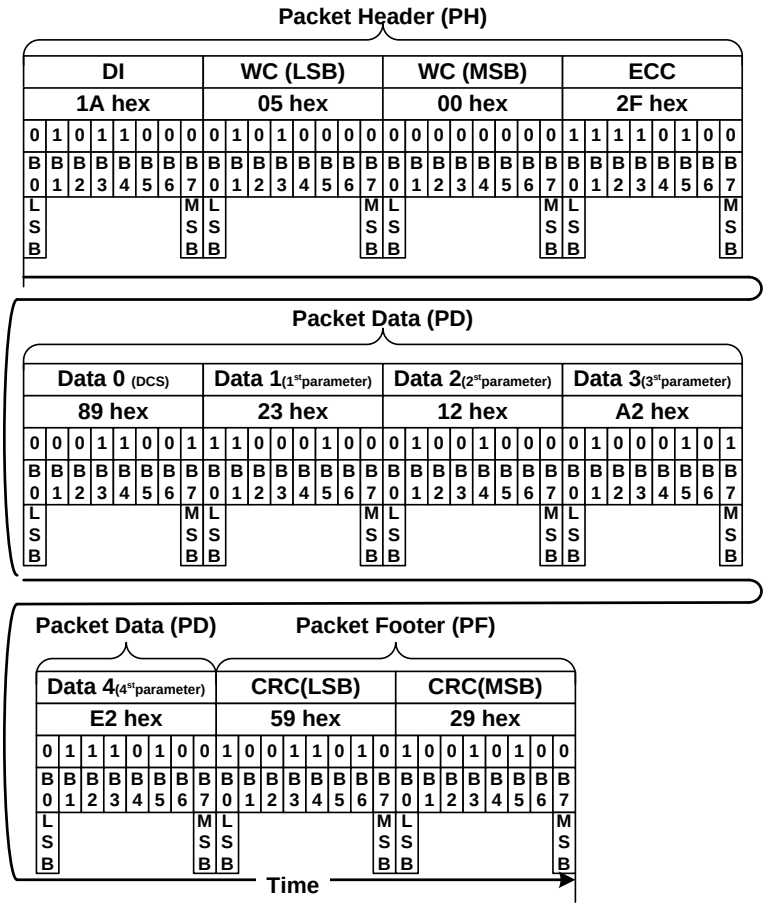
DCS Read Short Response,2 Bytes Returned (DCSRR2-S) -Example

Generic Read Long Response (GENRR-L), Data Type = 01 1010(1Ah)

"Generic Read Long Response" (GENRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 01 1010b), from the display module to the MCU. "Generic Read Long Response" (GENRR-L) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module. Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 01 1010b
- Word Count (WC)
  - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: 89h
  - Data 1: 23h
  - Data 2: 12h
  - Data 3: A2h
  - Data 4: E2h
- Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.



Generic Read Short Response, 1 Byte Returned (GENRR1-S), Data Type = 01 0001(11h)

"Generic Read Short Response, 1 Byte Returned" (GENRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0001b), from the display module to the MCU. "Generic Read Short Response, 1 Byte Returned" (GENRR1-S) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 01 0001b

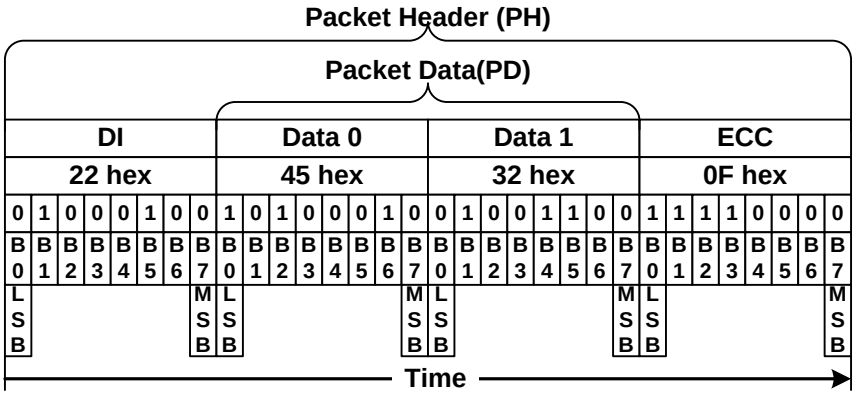
• Packet Data (PD):

  • Data 0: 45h

  • Data 1: 00h (Always)

• Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.



Generic Read Short Response,1 Byte Returned (GENRR1-S)-Example

Generic Read Short Response, 2 Bytes Returned (GENRR2-S), Data Type = 01 0010(12h)

"Generic Read Short Response, 2 Bytes Returned" (GENRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0010b), from the display module to the MCU. "Generic Read Short Response, 2 Bytes Returned" (GENRR2-S) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

• Data Identification (DI)

  • Virtual Channel (VC, DI[7…6]): 00b

  • Data Type (DT, DI[5…0]): 01 0010b

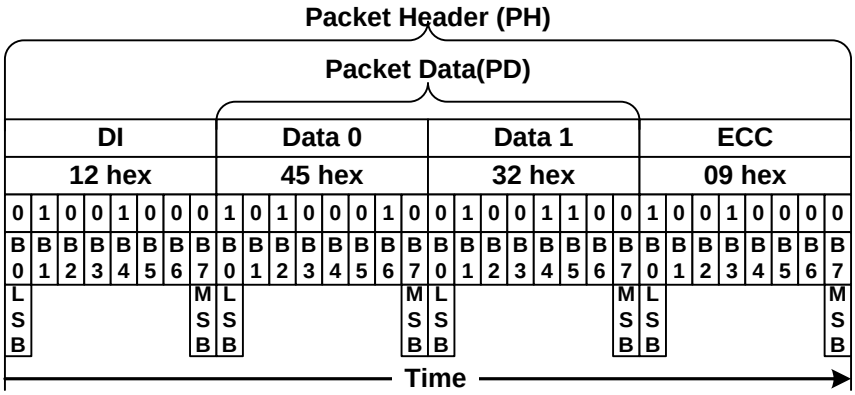
• Packet Data (PD):

  • Data 0: 45h

  • Data 1: 32h

• Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.



Generic Read Short Response, 2 Bytes Returned (GENRR2-S)-Example

8.7.2.3.3 COMMUNICATION SEQUENCES

8.7.2.3.3.1 GENERAL

The communication sequences can be done on interface or packet levels between the MCU and the display module. See chapters “Interface Level Communication” and “Packet Level Communication”.

This communication sequence description is for DSI data lanes and it has been assumed that the needed low level communication is done on DSI clock lanes (DSI-CLK+/-) automatically.

Functions of the interface level communication is described on the following table.

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop state
	LPDT	Low power data transmission
	ULPS	Ultra-Low power state
	RAR	Remote application reset
	TEE	Tearing effect event
	ACK	Acknowledge (No error)
	BTA	Bus turnaround
High Speed	HSDT	High speed data transmission

Table 21 Interface Level Communication

Functions of the packet level communication are described on the following table.

Packet Sender	Abbreviation	Packet Size	Packet Description
MCU	DCSW1-S	SPa	DCS Write,1 Parameter
	DCSWN-S	SPa	DCS Write, No parameter
	DCSW-L	LPa	DCS Write,Long
	DCSRN-S	SPa	DCS Read,No Parameter
	SMRPS-S	SPa	Set maximum return packet size
	NP-L	LPa	Null packet, No data
Display Module	AwER	SPa	Acknowledge with error report
	DCSRR-L	LPa	DCS Read, Long Response
	DCSRR1-S	SPa	DCS Read, Short Response
	DCSRR2-S	SPa	DCS Read, Short Response

Table 22 Packet Level Communication

8.7.2.3.3.2 SEQUENCES

DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” is defined on chapter “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” and example sequences, how this packet is used, is described on following tables.

DCS Write,1 Parameter Sequence – Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write,1 Parmeter Sequence – Example2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

DCS Write, 1 Parameter Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error=>goto line8 If error=goto line 13
7						
8	-	-	<=	ACK	-	No error
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	End
12						
13	-	-	<=	LPDT	AwER	Error report
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	
16	-	LP-11	=>	-	-	End

DCS Write, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” is defined on chapter “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” and example sequences, how this packet is used, is described on following tables.

DCS Write,No Parameter Sequence-Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write,No Parmeter Sequence – Example2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

DCS Write, No Parameter Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error=>goto line8 If error=goto line 13
7						
8	-	-	<=	ACK	-	No error
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	End
12						
13	-	-	<=	LPDT	AwER	Error report
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	
16	-	LP-11	=>	-	-	End

DCS Write Long Sequence

A Long Packet (LPa) of “Display Command Set (DCS) Write Long (DCSW-L)” is defined on chapter “Display Command Set (DCS) Write Long (DCSW-L)” and example sequences, how this packet is used, is described on following tables.

DCS Write, Long Sequence-Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, Long Sequence – Example2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

DCS Write, Long Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error=>goto line8 If error=goto line 13
7						
8	-	-	<=	ACK	-	No error
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	End
12						
13	-	-	<=	LPDT	AwER	Error report
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	
16	-	LP-11	=>	-	-	End

DCS Read, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” is defined on chapter “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” and example sequences, how this packet is used, is described on following tables.

DCS Read, No Parameter Sequence – Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>		-	Start
2	SMRPS-S	HSDT	=>		-	Define how many data byte is wanted to read: 1 byte
3	DCSRN-S	HSDT	=>		-	Wanted to get a response ID1 (DAh)
4	EoTP	HSDT	=>		-	End of Transmission Packet
5	-	LP-11	=>		-	
6	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
7	-	-	<=	LP-11	-	If no error=>goto line 9 If error=> goto line 14 If error is corrected by ECC =>go to line 19
8						
9	-	-	<=	LPDT	DCSRR1-S	Responsed 1 byte return
10	-	-	<=	LP-11	-	
11	-	BTA	<=>	BTA	-	Interface control change from the Display module to the MCU
12	-	LP-11	=>	-	-	End
13						
14	-	-	<=	LPDT	AwER	Error report
15	-	-	<=	LP-11	-	
16	-	BTA	<=>	BTA	-	Interface Control change from the Display module to the MCU
17	-	LP-11	=>	-	-	End
18						
19	-	-	<=	LPDT	DCSRR1-S	Responsed 1 byte return
20	-	-	<=	LPDT	AwER	Error Report (Error is Corrected by ECC)
21	-	-	<=	LP-11	-	
22	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
23	-	LP-11	=>	-	-	End

Null Packet, No Data Sequence

A Long Packet (LPa) of “Null Packet, No Data (NP-L)” is defined on chapter “Null Packet, No Data (NP-L)” and example sequences, how this packet is used, is described on following tables.

Null Packet, No Parameter Sequence - Example

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	NP-L	HSDT	=>	-	-	Only high speed data transmission Is used
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

End of Transmission Packet

A Short Packet (SPa) of “End of Transmission (EoT)” is defined on chapter “End of Transmission Packet (EoT)” and an example sequences, how this packet is used, is described on following tables.

End of Transmission Packet – Example

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	NP-L	HSDT	=>	-	-	Only high speed data transmission Is used
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

8.7.2.4 Video Mode Communication

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

8.7.2.4.1 TRANSMISSION PACKET SEQUENCES

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's timing requirements dictate which format is appropriate. In the following sections, Burst Mode refers to time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are used throughout the following sections:

• Non-Burst Mode with Sync Pulses – enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.

• Non-Burst Mode with Sync Events – similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.

• Burst mode – RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral. To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. It is recommended to return to LP state once per scan-line during the horizontal blanking time. Regardless of the frequency of BLLP periods, the host processor is responsible for meeting all documented peripheral timing requirements. Note, at lower frequencies BLLP periods will approach, or become, zero, and burst mode will be indistinguishable from non-burst mode.

During the BLLP the DSI Link may do any of the following:

• Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX

• Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode

• Transmit one or more non-video packets from the host processor to the peripheral using HS Mode

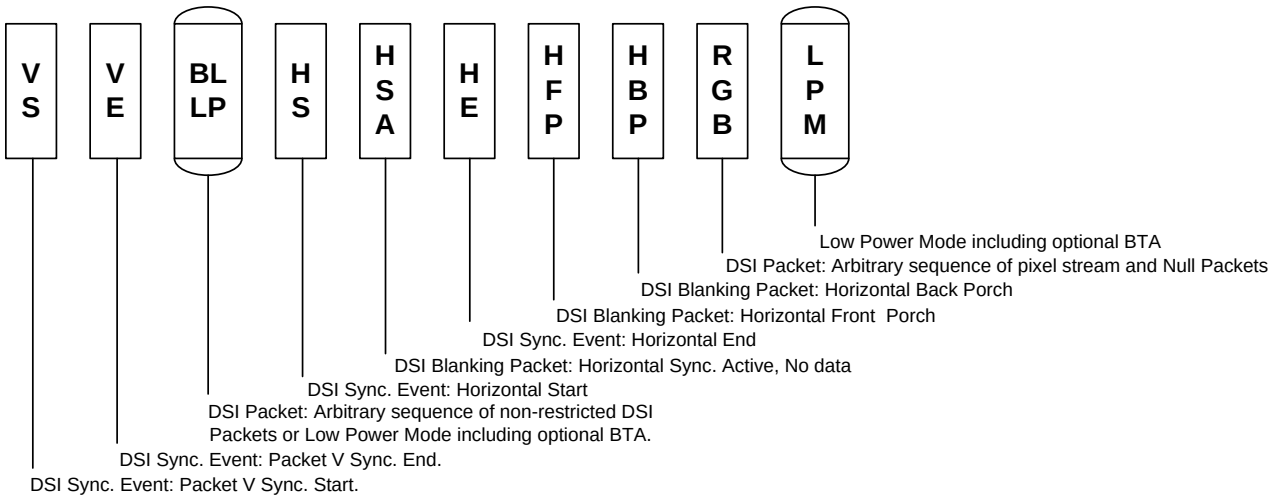
• If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode

• Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VS; all other lines shall start with HS. This is also true in the special case when VSA+VBP=0. Note that the position of synchronization packets, such as VS and HS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Normally, RGB pixel data is sent with one full scan line of pixels in a single packet. If necessary, a horizontal scan-line of active pixels may be divided into two or more packets. However, individual pixels shall not be split across packets.

Transmission packet components used in the figures in this section are defined in Figure below unless otherwise specified.



DSI Video Mode Interface Timing Legend

If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

There are two limitation for MIPI Video mode 2 Lane:

(1) The packet number for H-porch or 1-line data should be even.

(2) Packet Pixel Stream should be start at Lane0.

8.7.2.4.2 NON-BURST MODE WITH SYNC PULSES

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure below.

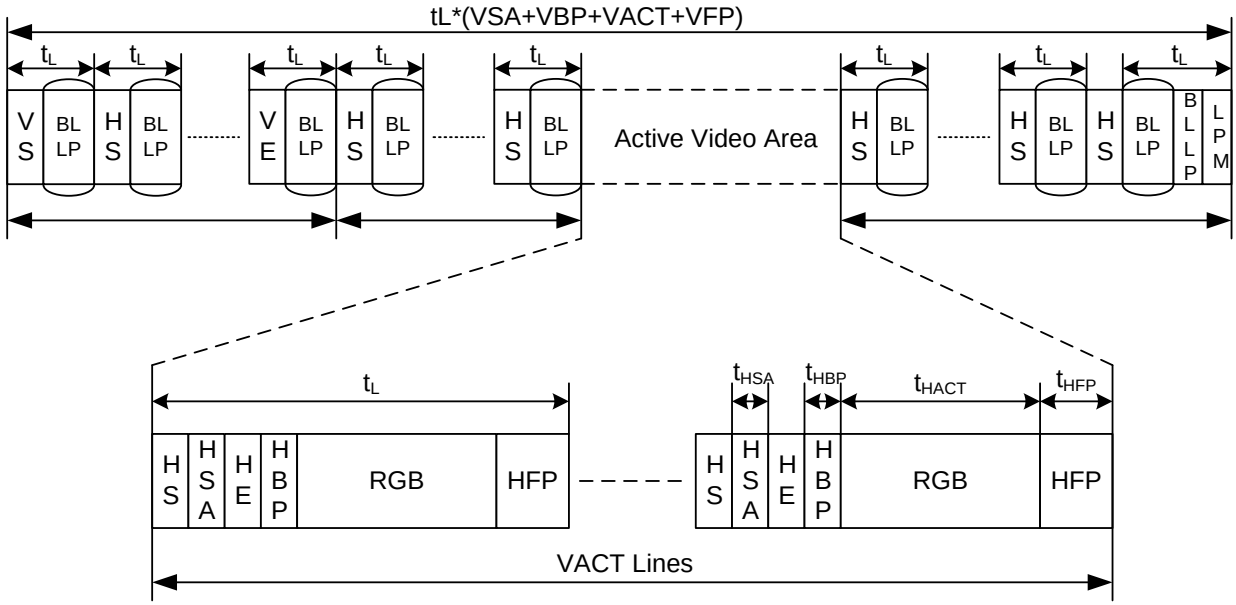


Figure 83 DSI Video Mode Interface Timing: Non-Burst Transmission with Sync Start and End

Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

8.7.2.4.3 NON-BURST MODE

This mode is a simplification of the format described in section 5.3.2.4.2 “Non-Burst Mode with Sync Pulse” .Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. Pixels are transmitted at the same rate as they would in a corresponding parallel display interface such as DPI-2. An example of this mode is shown in Figure below.

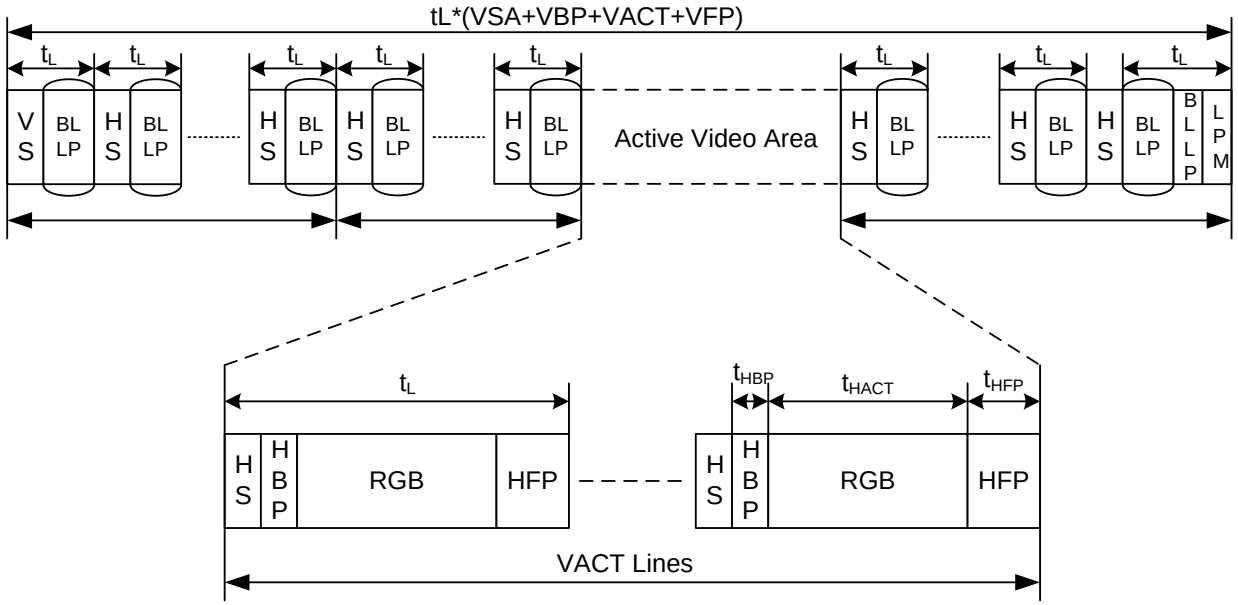


Figure 84 DSI Video Mode Interface Timing: Non-burst Transmission

As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

8.7.2.4.4 BURST MODE

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction. There may be a line buffer or similar memory on the peripheral to accommodate incoming data at high speed. Following HS pixel data transmission, the bus goes to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in Figure below.

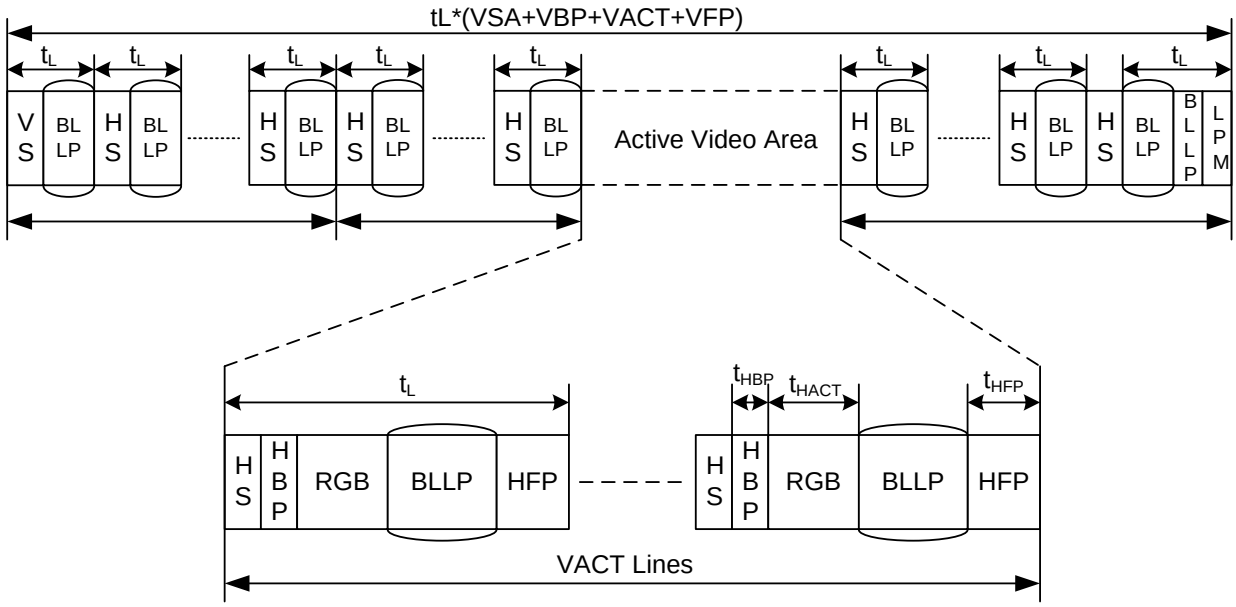


Figure 85 DSI Video Mode Interface Timing: Burst Transmission

Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

9 POWER ON/OFF SEQUENCE

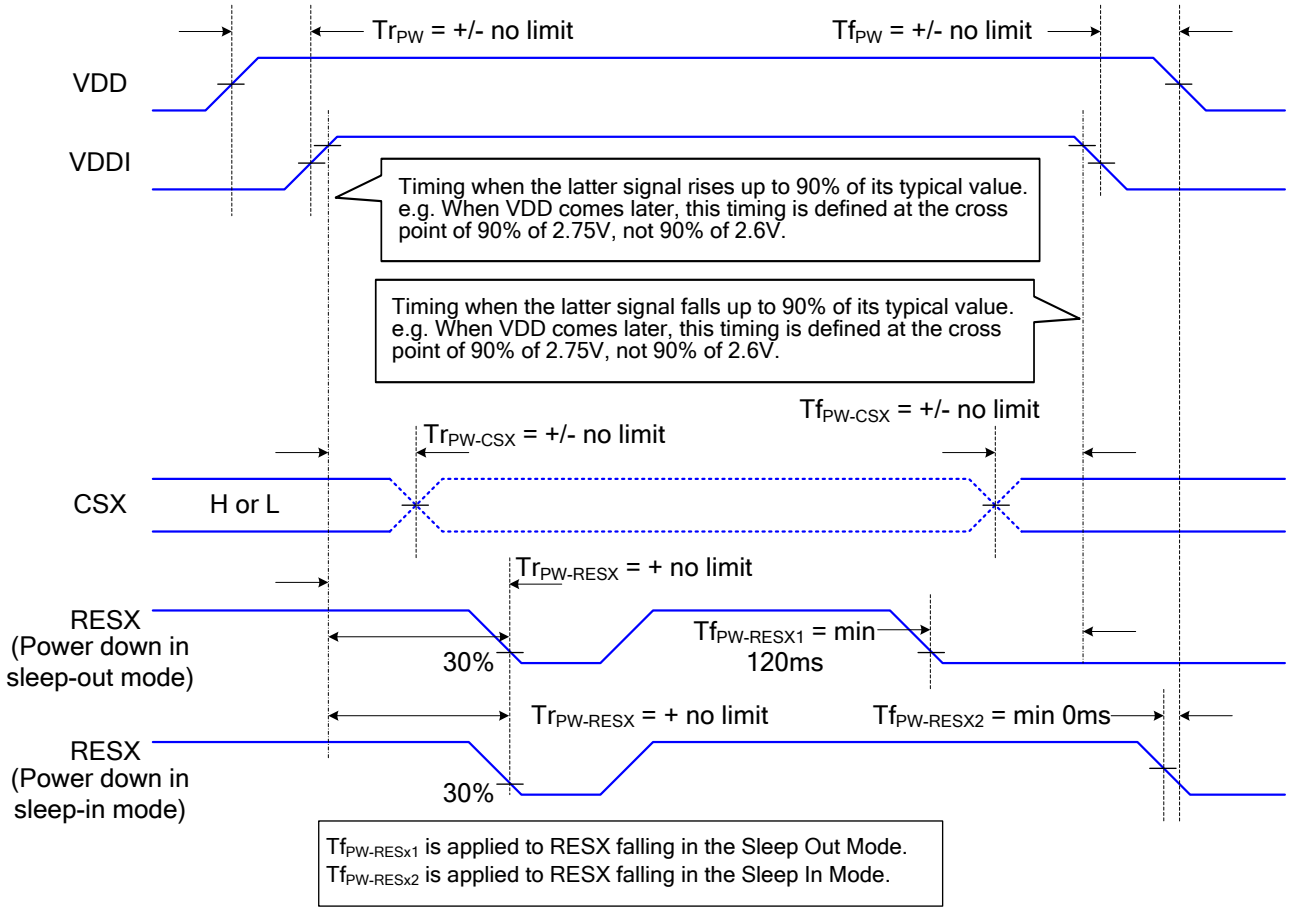
VDDI and VDDA can be applied or powered down in any order. During the Power Off sequence, if the LCD is in the Sleep Out mode, VDDA and VDDI must be powered down with minimum 120msec. If the LCD is in the Sleep In mode, VDDA and VDDI can be powered down with minimum 0msec after the RESX is released.

CSX can be applied at any timing or can be permanently grounded. RESX has high priority over CSX.

Notes:

1. There will be no damage to the ST7701S if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between the end of Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.
4. If the RESX line is not steadily held by the host during the Power On Sequence as defined in Sections 9.1 and 9.2, then it will be necessary to apply the Hardware Reset (RESX) after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.

The power on/off sequence is illustrated below



9.1 Uncontrolled Power Off

The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display (blank display) and remains blank until “Power On Sequence” powers it up.

10 POWER LEVEL DEFINITION

10.1 Power Level

7 level modes are defined they are in order of maximum power consumption to minimum power consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show maximum 16.7M colors.

2. Partial Mode On, Idle Mode Off, Sleep Out

In this mode, part of the display is used with maximum 16.7M colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode.

In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. Only the MPU interface and registers are working with VDDI power supply.

6. Deep Standby Mode.

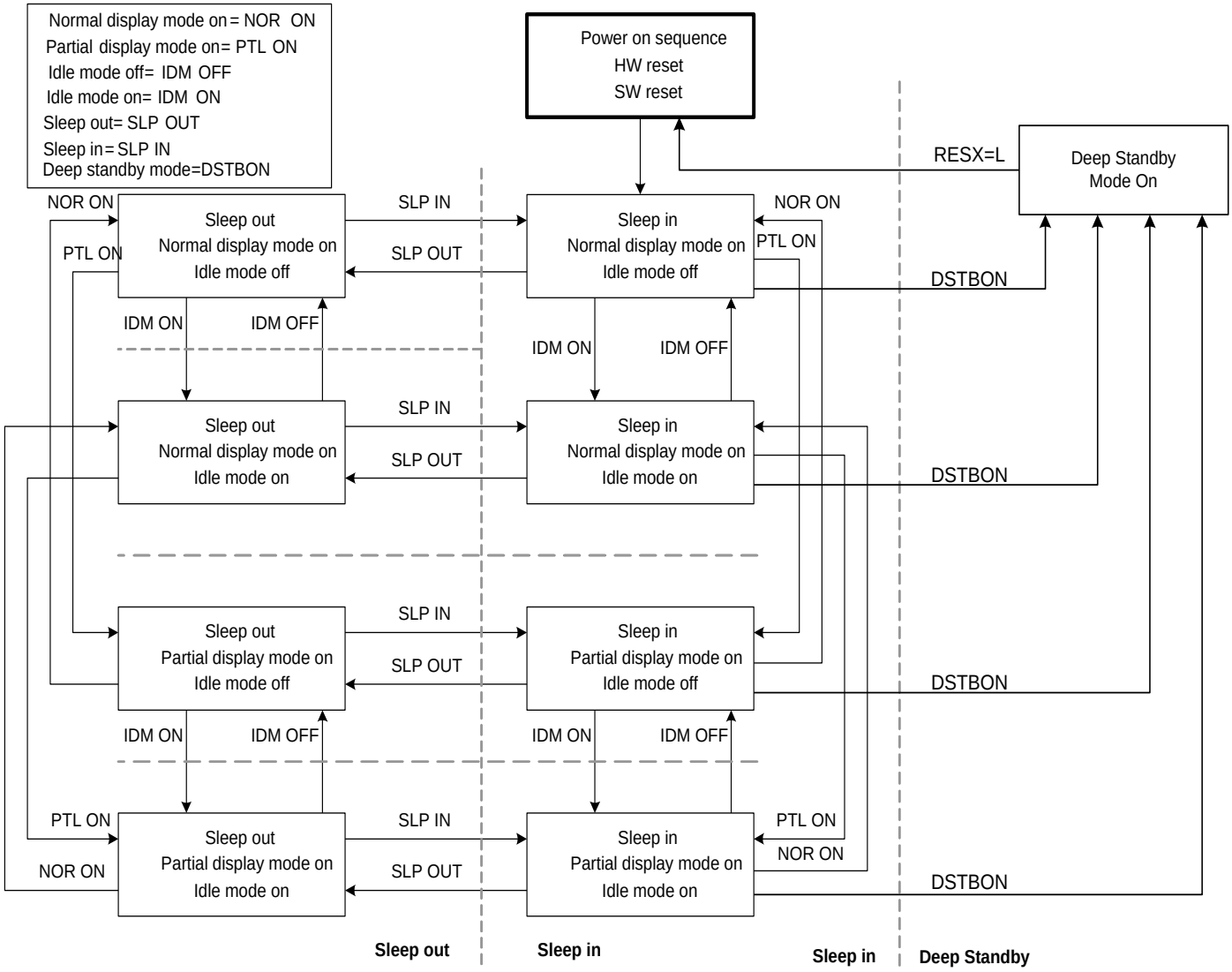
In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. The MPU interface and registers are not working.

7. Power Off Mode

In this mode, VDDI and VDDA/VDDB are removed.

NOTE: Transition between mode 1~5 is controllable by MPU commands. Mode 6 is entered for power saving with both power supplies for I/O and analog circuits and can be exited by hardware reset only (RESX=L). Mode 7 is entered only when both power supplies for I/O and analog circuits are removed.

10.2 Power Flow Chart



NOTES:

1) There is not any abnormal visual effect when there is changing from one power mode to another power mode.

2) There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode

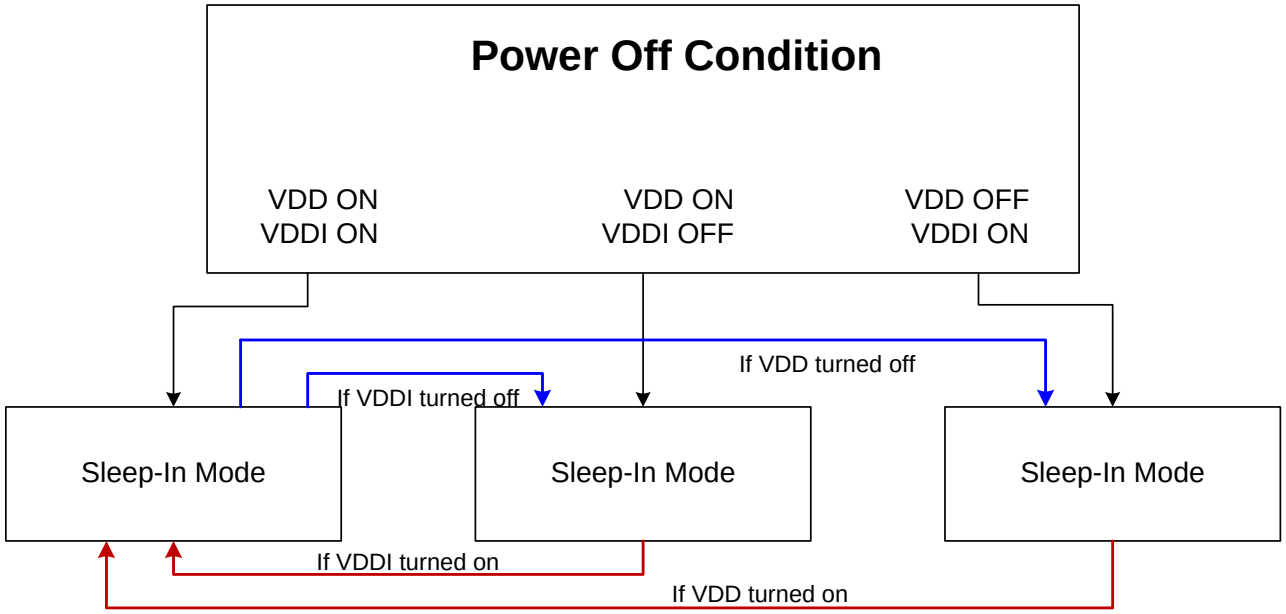
The following table represents the Registers its mode state.

Mode	Register	Control	
		Enter	Exit
Sleep in mode	Keep	Command	
Deep-standby mode	Loss	Command	Reset pin
Reset=L	Keep(Default Value)	Reset (H/W)	

The condition for irregular power off mode is shown below.

Power Off Mode	VDD	VDDI	RESX	I/O
Mode 1	ON	OFF	High to Low	Low
Mode 2	OFF	ON	High to Low	Low

Note: VDD means VDDA, VDDB



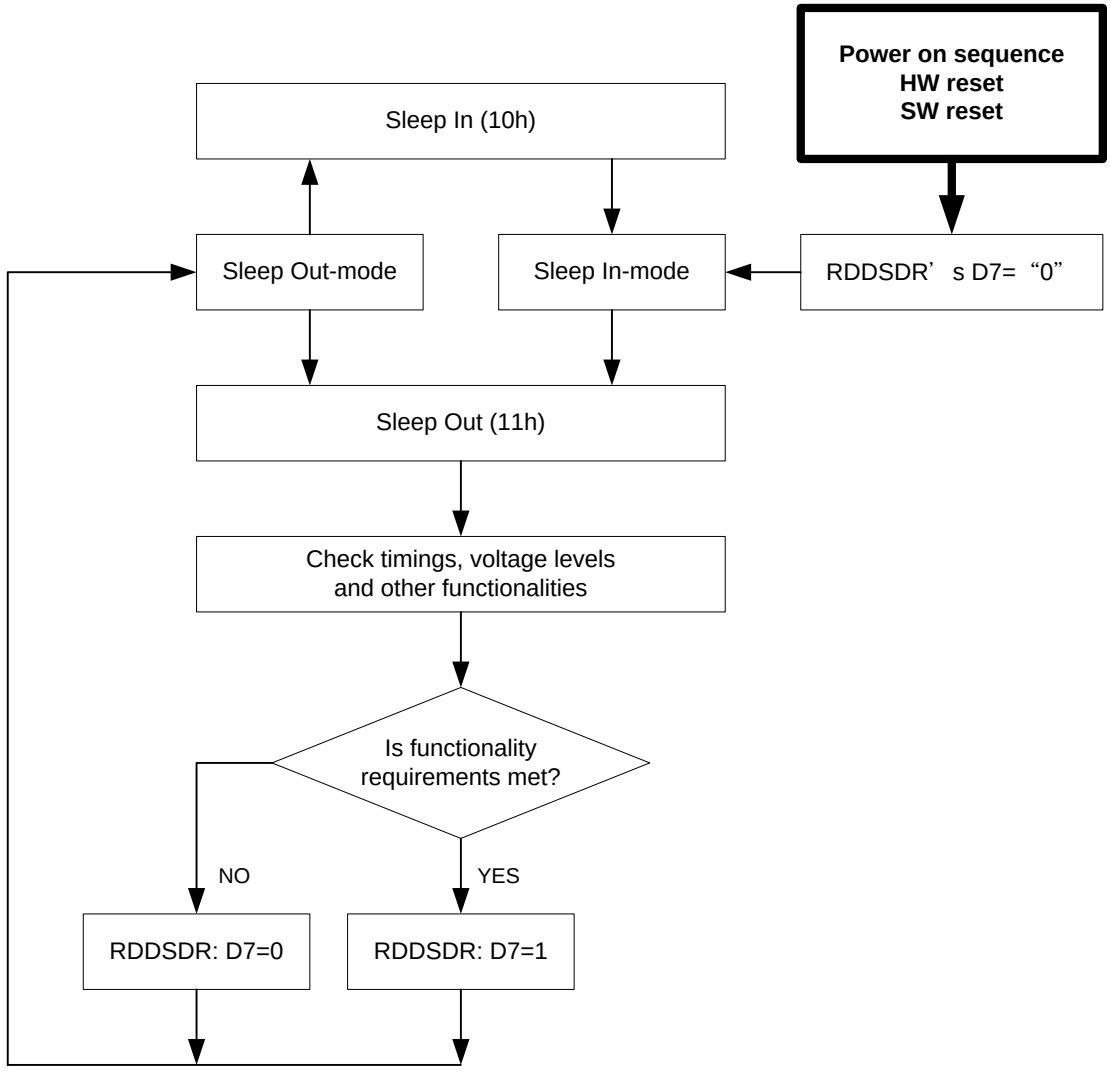
10.3 Sleep Out –Command and self-diagnostic functions of the display module

10.3.1 Register loading Detection

Sleep Out-command is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from ROM to registers of the display controller is working properly.

There are compared factory values of the ROM and register values of the display controller by the display controller (1st step: compare register and ROM values, 2nd step: loads ROM values to registers). If those both values (ROM and register values) are same, there is inverted (= increased by 1) a bit, which is defined in command RDDSDR (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= not increased by 1).

The flow chart for this internal function is following:

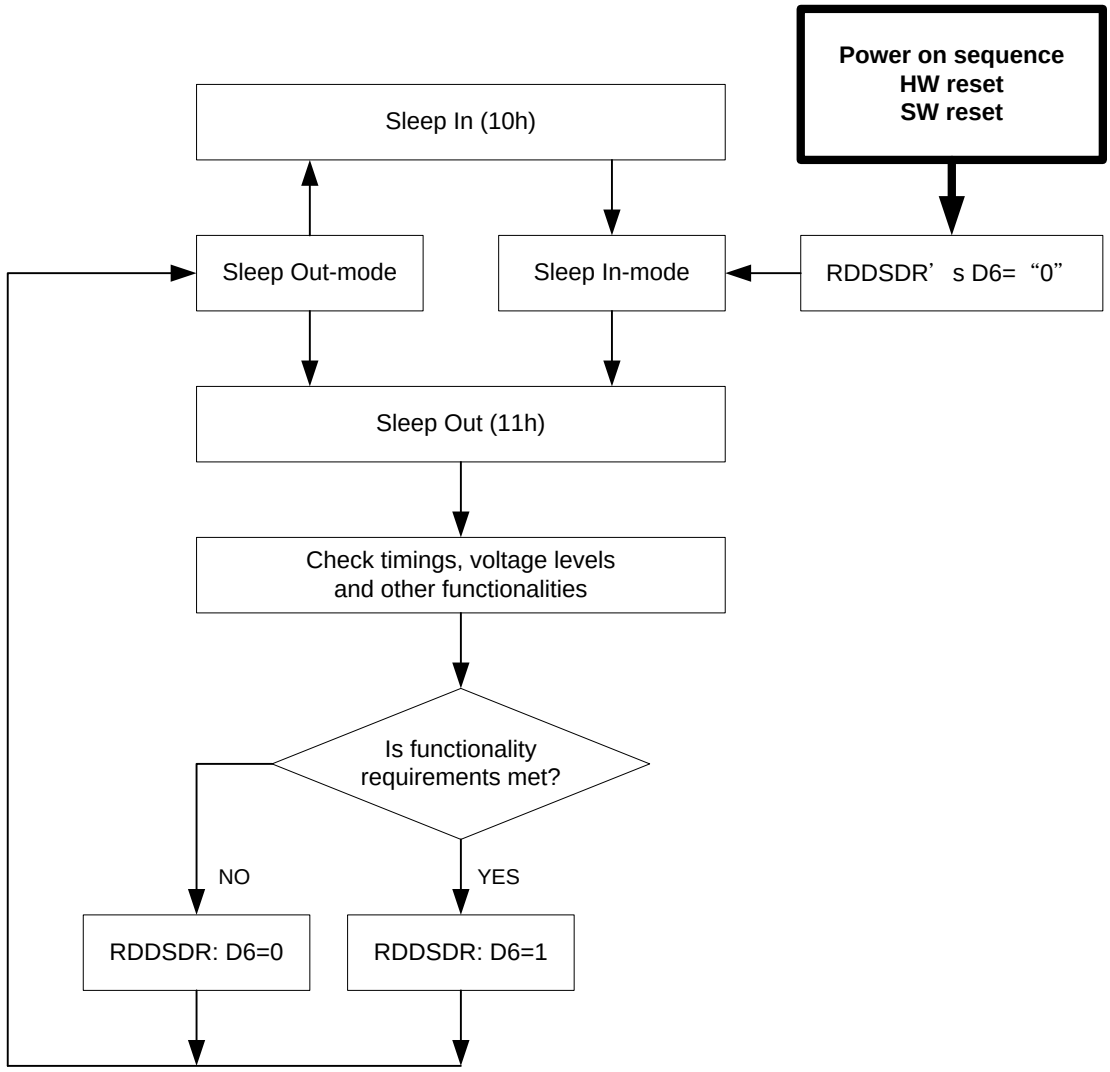


10.3.2 Functionality Detection

Sleep Out-command is a trigger for an internal function of the display module.

The internal function (= the display controller) is comparing if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, bit-6 of RDDSDR is set to 1, which defined in command Read Display Self-Diagnostic Result (RDDSDR). The used bit of this command is D6. If functionality requirement is not same, this bit (D6) is set to 0.

The flow chart for this internal function is following:



11 GAMMA CORRECTION

ST7701S incorporate the gamma correction function to display 16M colors for the LCD panel. The gamma correction is performed with 3 groups of registers, which are gradient adjustment, contrast adjustment and fine- adjustment registers for positive and negative polarities, and RGB can be adjusted individually.

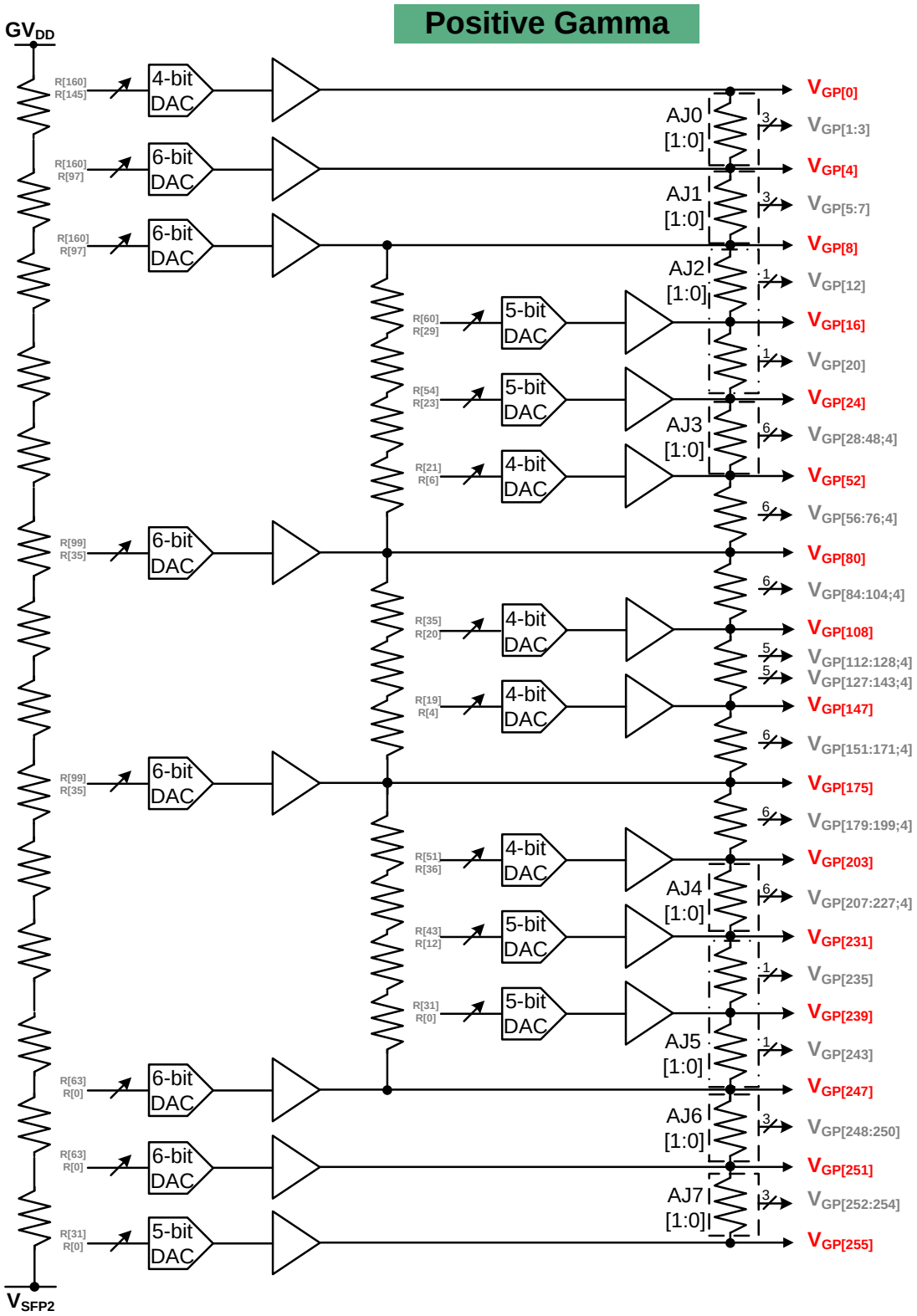


Figure 86 Gray scale Voltage Generation (Positive)

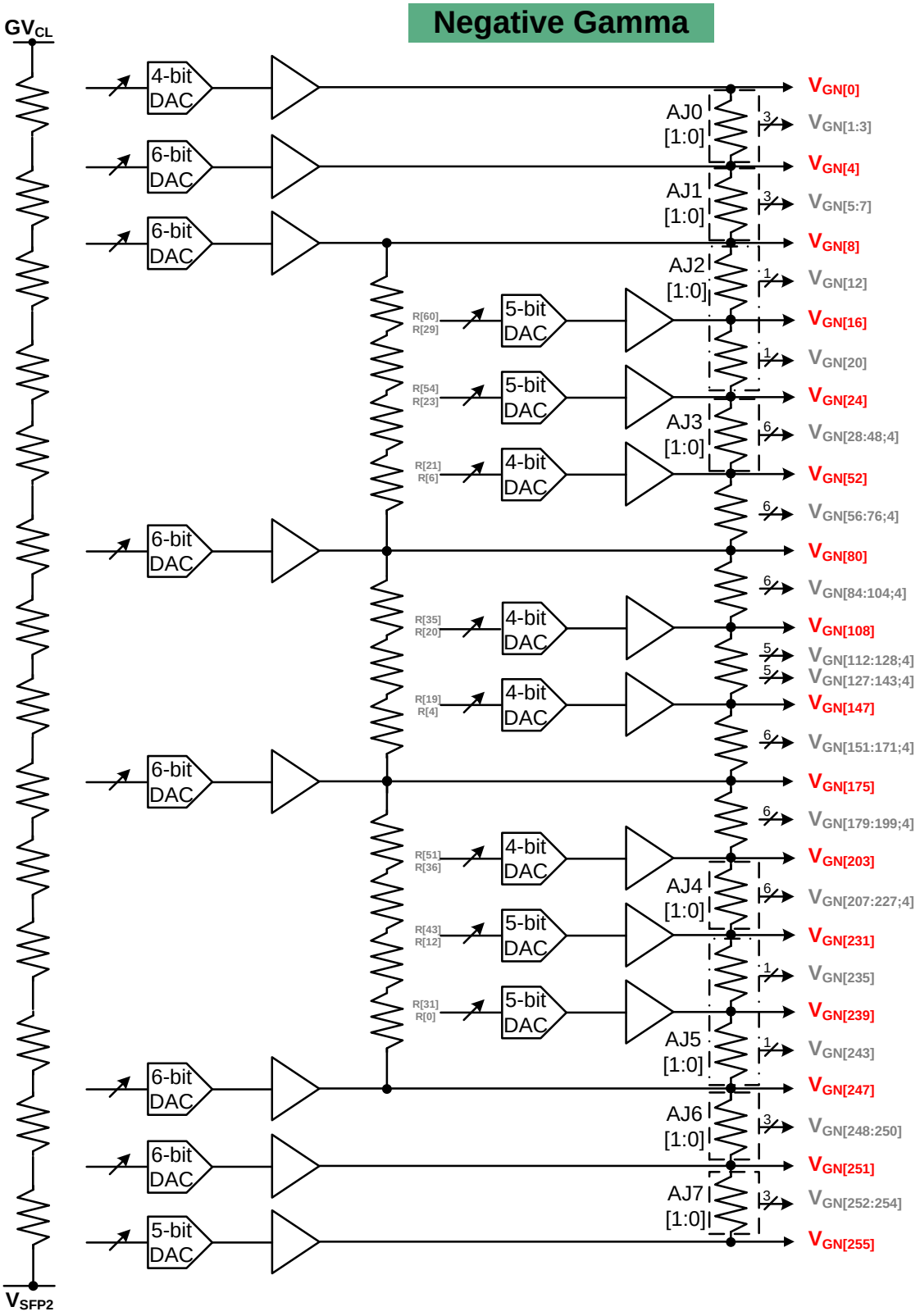


Figure 87 Gray scale Voltage Generation (Positive)

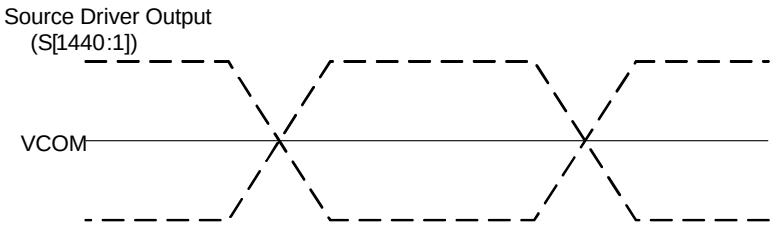


Figure 88 Relationship between Source Output and VCOM

Percentage adjustment:

AJ0P[1:0], AJ1P[1:0], AJ2P[1:0], AJ3P[1:0], AJ0N[1:0], AJ1N[1:0], AJ2N[1:0], AJ3N[1:0], these register are used to adjust the voltage level of interpolation point. The following table is the detail description.

AJ0P[1:0]/AJ0N[1:0]:

	00h	01h	02h	03h
VP1/VN1	64%	75%	70%	53%
VP2/VN2	27%	50%	41%	17%
VP3/VN3	9%	25%	15%	3%
VP5/VN5	75%	75%	88%	88%
VP6/VN6	50%	50%	58%	58%
VP7/VN7	25%	25%	29%	29%

AJ1P[1:0]/AJ1N[1:0]:

	00h	01h	02h	03h
VP12/VN12	50%	54%	50%	60%
VP20/VN20	50%	44%	50%	42%
VP28/VN28	86%	71%	80%	66%
VP32/VN32	71%	57%	63%	49%
VP36/VN36	57%	40%	49%	34%
VP40/VN40	43%	29%	34%	23%
VP44/VN44	29%	17%	20%	14%
VP48/VN48	14%	6%	9%	6%

AJ2P[1:0]/AJ2N[1:0]:

	00h	01h	02h	03h
VP207/VN207	86%	86%	86%	89%
VP211/VN211	71%	71%	77%	80%
VP215/VN215	57%	60%	63%	69%
VP219/VN219	43%	43%	46%	51%
VP223/VN223	29%	34%	31%	37%
VP227/VN227	14%	17%	14%	20%
VP235/VN235	50%	56%	47%	47%
VP243/VN243	50%	50%	50%	53%

AJ3P[1:0]/AJ3N[1:0]:

	00h	01h	02h	03h
VP248/VN248	75%	75%	71%	71%
VP249/VN249	50%	50%	42%	42%
VP250/VN250	25%	25%	13%	13%
VP252/VN252	91%	75%	85%	97%
VP253/VN253	73%	50%	59%	83%
VP254/VN254	36%	25%	30%	48%

Table 23 voltage level percentage adjustment description

11.1 Gray voltage generator for digital gamma correction

ST7701S digital gamma function can implement the RGB gamma correction independently. ST7701S utilizes look-up table of digital gamma to change ram data, and then display the changed data from source driver. The following diagram shows the data flow of digital gamma.

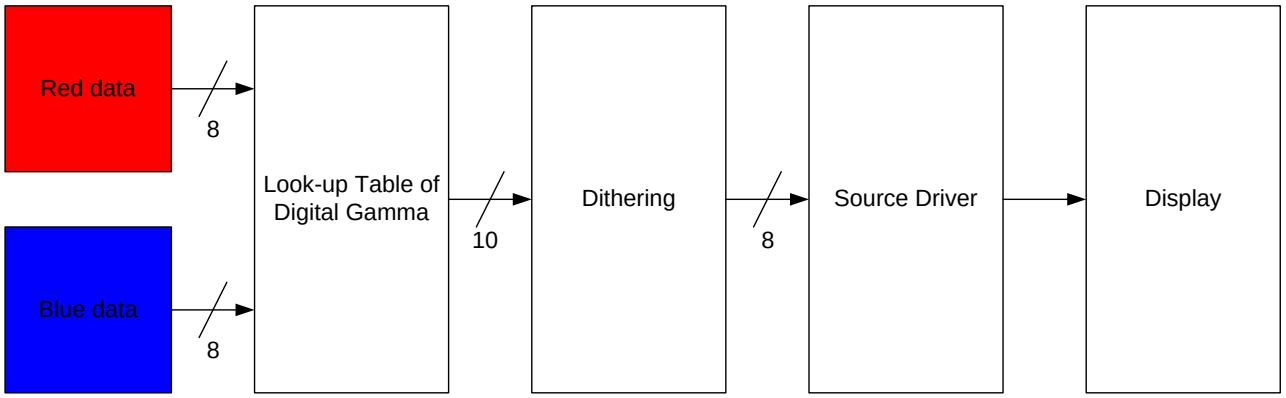


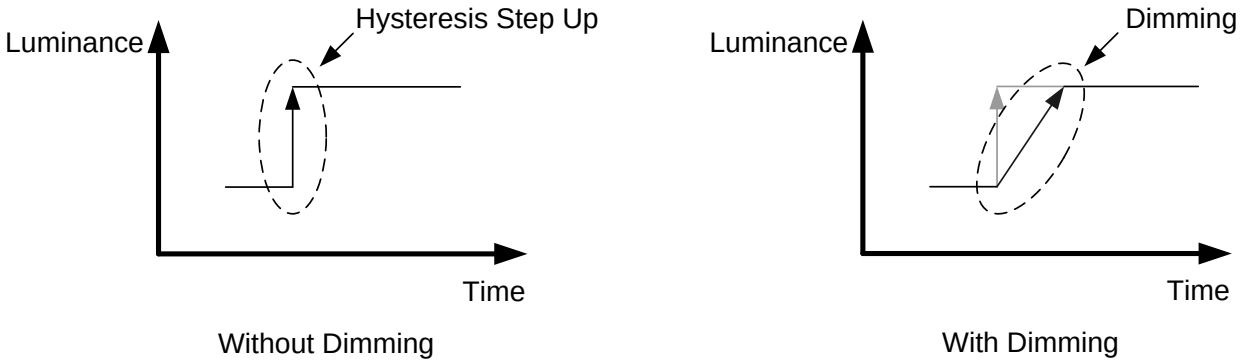
Figure 89 Block diagram of digital gamma

There are 2 registers and each register has 260 bytes to set R, G, B gamma independently. When bit DGMEN be set to 1, R and B gamma will be mapped via look-up table of digital gamma to gray level voltage.

11.2 Display Dimming

General Description

A dimming function (how fast to change the brightness from old to new level and what are brightness levels during the change) is used when changing from one brightness level to another. This dimming function curve is the same in increment and decrement. The basic idea is described below.



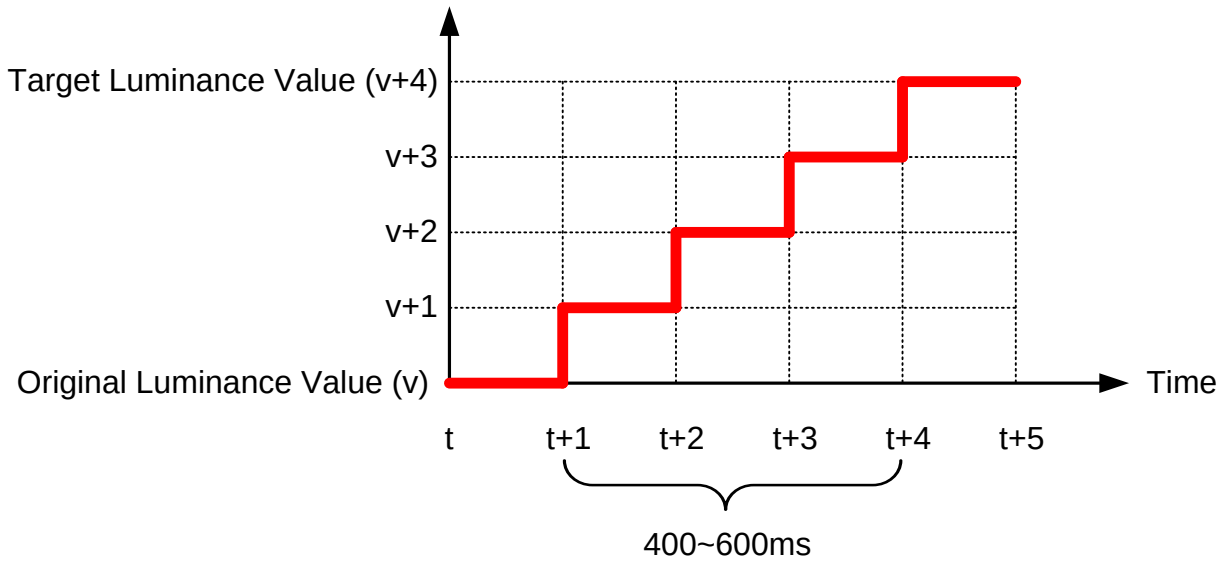
Dimming function can be enable and disable. See “Write CTRL Display (53h)” (bit DD) for more information.

Dimming Requirement

Dimming function in the display module should be implemented so that 400-600ms is used for the transition between the original brightness value and the target brightness value. The transferring time steps between these two brightness values are equal making the transition linear.

The dimming function is working similarly in both upward and downward directions.

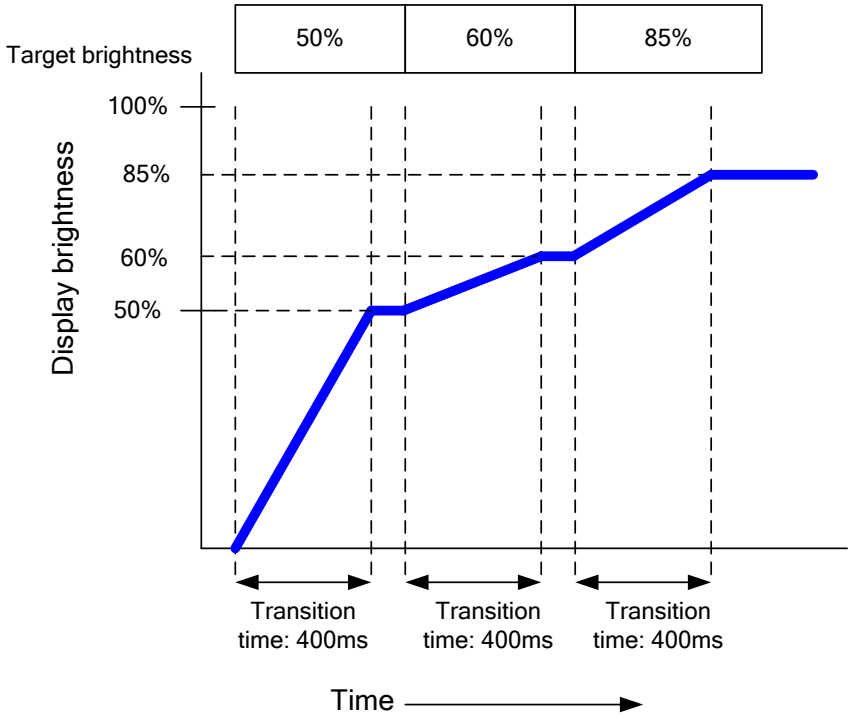
An upward example is illustrate below



Definition of brightness transition time

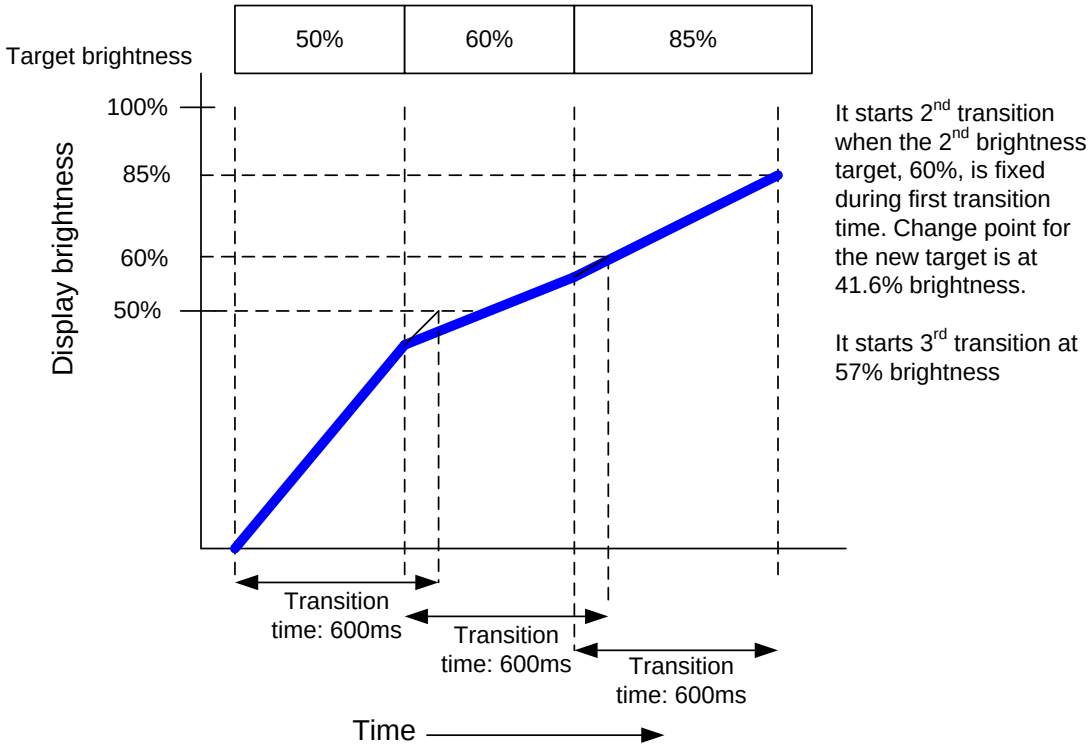
- Shorter transition time than 500ms.

  There is some stable time between transitions. Below drawing is for transition time: 400ms.



- Longer transition time than 500ms

  There is no any stable time between transitions. Below drawing is for transition time: 600ms.



It starts 2nd transition when the 2nd brightness target, 60%, is fixed during first transition time. Change point for the new target is at 41.6% brightness.

It starts 3rd transition at 57% brightness

11.3 Content Adaptive Brightness Control (CABC)

Definition of CABC

A Content Adaptive Brightness Control function can be used to reduce the power consumption of the luminance source. Content adaptation means that content gray level scale can be increased while simultaneously lowering brightness of the backlight to achieve same perceived brightness. The adjusted gray level scale and thus the power consumption reduction

Definition of Modes and target power reduction ratio:

- Off mode: Content Adaptive Brightness Control functionality is totally off.
- UI [User interface] image mode: Optimized for UI image. It is kept image quality as much as possible. Target power consumption reduction ratio: 10% or less.
- Still picture mode: Optimized for still picture. Some image quality degradation would be acceptable. Target power consumption reduction ratio: more than 30%.
- Moving image mode: Optimized for moving image. It is focused on the biggest power reduction with image quality degradation. Target power consumption reduction ratio: more than 30%.

Note 1: Updating partial area of the image data should be supported by CABC functionality.
Note 2: Processing power consumption of CABC should be minimized.

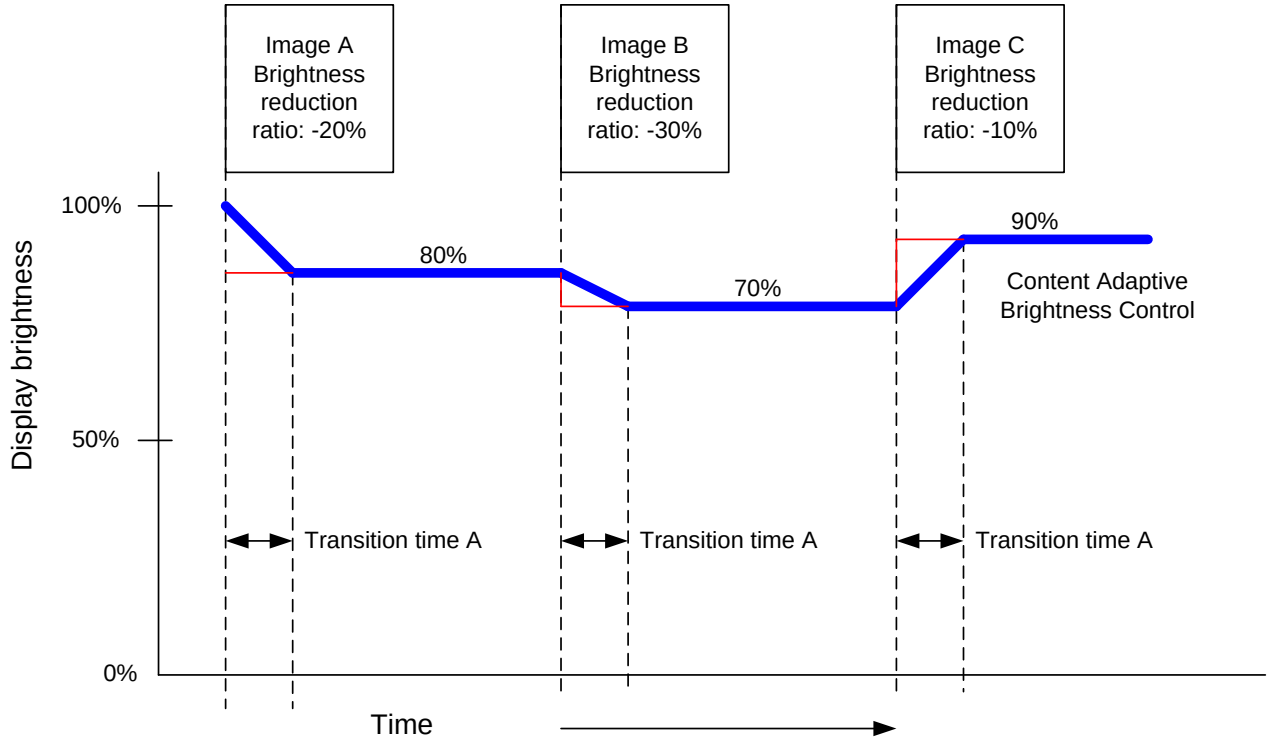
The transition time for dimming function is illustrated below.

- Content Adaptive Brightness Control

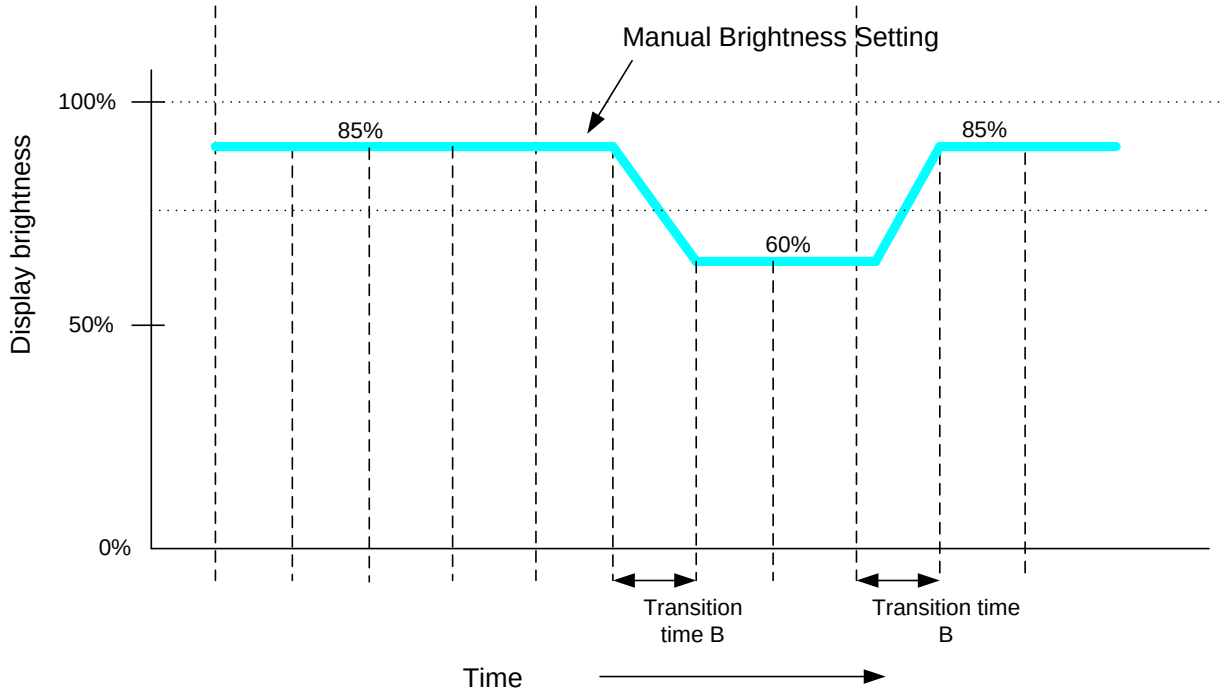
Display brightness is changed, according to the image contents. The following graph mentions the case of displaying three different images.

- Image A: -20% brightness reduction
- Image B: -30% brightness reduction
- Image C: -30% brightness reduction

Transition time from the previous image to the current displayed image is “transition time A”.



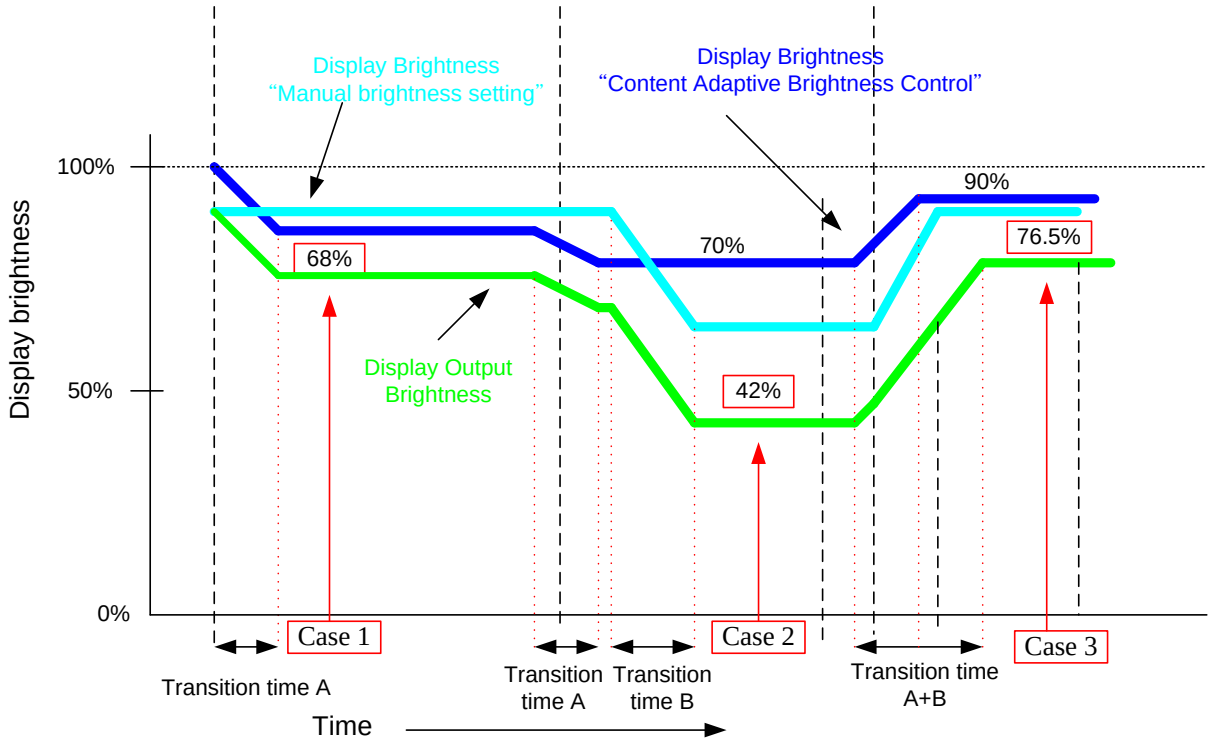
- Manual brightness setting and Dimming function



- Combine Display brightness

Green line in the following graph is for the output brightness of display. It is combined with both display brightness, which are defined in the above graphs.

Maximum transition time is transition time A+B.



Brightness level calculates with the following formula.

Display Output brightness = Manual Brightness setting * CABC brightness ratio

	Manual Brightness setting	Brightness ratio [CABC]	Display Output brightness
Case 1	85%	80%	68%
Case 2	60%	70%	42%
Case 3	85%	90%	76.5%

Transition time from the current brightness to target brightness is A+B in the worst case.

Minimum brightness setting of CABC function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with the LABC or manual brightness setting, display brightness is too dark. It must affect to image quality degradation. CABC minimum brightness setting is to avoid too much brightness reduction. When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. If CABC algorithm works without any abnormal visual effect, image processing function can operate even when the brightness can not be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

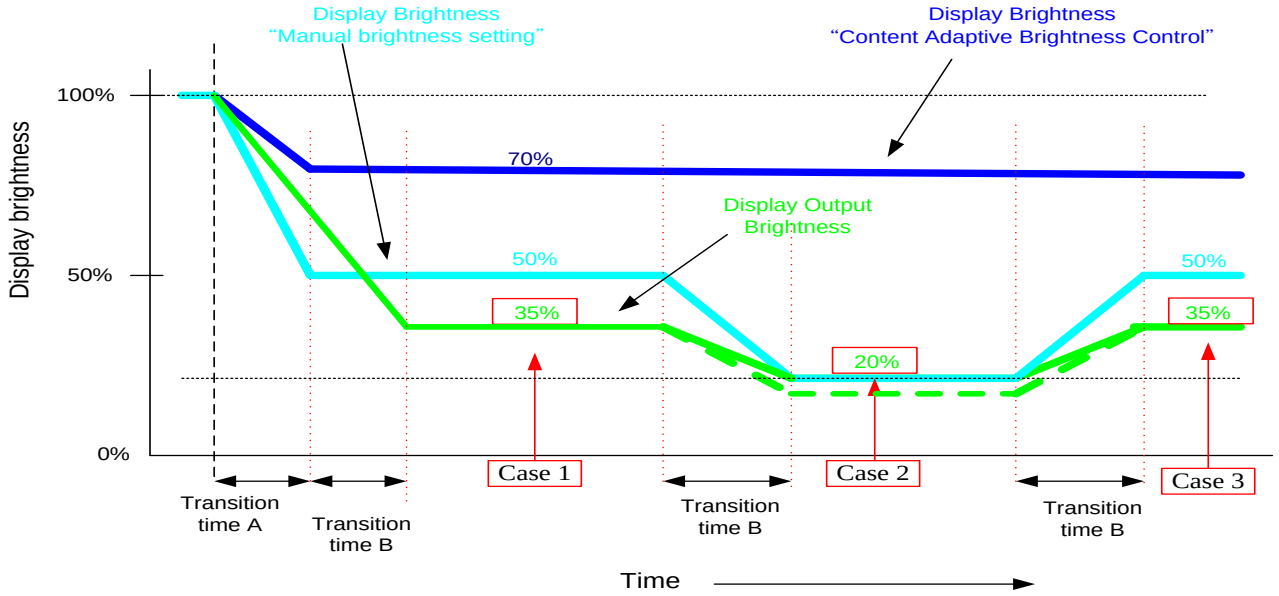
When display brightness is turned off (BCTRL=0 of the Write CTRL Display (53h)"), CABC minimum brightness setting is ignored. "Read CABC minimum brightness (5Fh)" always read the setting value of "Write CABC minimum brightness (5Eh)".

	WRCABC (55h)	Function	RDCABCMB (5Fh)	Image
Sleep-in	--	NA	WRCABCMB (5Eh)	--
CABC off	00b	Disable	WRCABCMB (5Eh)	Original
CABC on	01b/10b/11b	Enable	WRCABCMB (5Eh)	CABC modified

Brightness level calculates with the following formula.

Display Output Brightness = Manual brightness setting * CABC brightness ratio

Below drawing is for the explanation of the CABC minimum brightness setting.



CABC minimum brightness value = 51 (33h: 20% display brightness)

	Display Brightness [manual setting]	Brightness ratio [CABC]	Calculation result of the display brightness formula	Display Output Brightness	Image
Case 1	50%	70%	35%	35%	CABC modified
Case 2	20%	70%	14%	20%	CABC modified
Case 3	50%	70%	35%	35%	CABC modified

At the case 2, the calculation result of the display brightness is 14%. CABC minimum brightness value is set to 20% brightness. Actual display brightness is 20% as the CABC minimum brightness setting.

12 COMMAND

12.1 Command Transmission Mode on MIPI Interface

Command	MIPI Transmission Mode
Command Table1	LPDT / HSDT
Command Table2	LPDT

12.2 System Function Command Table 1

Instruction	Address		R/W/C	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Function
	MIPI	SPI-16											
NOP	00h	0000h	C	0	0	0	0	0	0	0	0	0	No operation
SWRESET	01h	0100h	C	0	0	0	0	0	0	0	0	1	Software reset
RDDID	04h	0400h	R	3	ID1[7:0]								ID1 read
		0401h			ID2[7:0]								ID2 read
		0402h			ID3[7:0]								ID3 read
RDNUMED	05h	0500h	R	1	ErrOver	Err[6:0]							Read No. of the Errors on DSI only
RDRED	06h	0600h	R	1	R_1st[7:0]								Read the first pixel of Color R
RDGREEN	07h	0700h	R	1	G_1st[7:0]								Read the first pixel of Color G
RDBLUE	08h	0800h	R	1	B_1st[7:0]								Read the first pixel of Color B
RDDPM	0Ah	0A00h	R	1	BSTON	0	0	SLPOUT	1	DISON	--	--	Read Display Power Mode
RDDMADCTL	0Bh	0B00h	R	1	--	--	--	ML	BGR	--	--	--	Read Display MADCTR
RDDCOLMOD	0Ch	0C00h	R	1	--	VIPF[2:0]		--	--	--	--	--	Read Display Pixel Format
RDDIM	0Dh	0D00h	R	1	--	--	INVON	ALPXLON	ALPXLOFF	GCS[2:0]			Read Display Image Mode
RDDSM	0Eh	0E00h	R	1	TEON	TELMD	--	--	--	--	--	--	Read Display Signal Mode
RDDSDR	0Fh	0F00h	R	1	RLD	FUND	0	0	--	--	--	--	Read Display Self-diagnostic result
SLPIN	10h	1000h	C	0	0	0	0	0	0	0	1	0	Sleep in
SLPOUT	11h	1100h	C	0	0	0	0	1	0	0	0	1	Sleep out
PTLON	12h	1200h	C	0	0	0	0	1	0	0	1	0	Partial mode on
NORON	13h	1300h	C	0	0	0	0	1	0	0	1	1	Normal display mode on
INVOFF	20h	2000h	C	0	0	0	1	0	0	0	0	0	Display inversion off (normal)
INVON	21h	2100h	C	0	0	0	1	0	0	0	0	1	Display inversion on
ALLPOFF	22h	2200h	C	0	0	0	1	0	0	0	1	0	All pixel off (black)
ALLPON	23h	2300h	C	0	0	0	1	0	0	0	1	1	All pixel on (white)
GAMSET	26h	2600h	W	1	--	--	--	--	GC[3:0]				Gamma curve select
DISPOFF	28h	2800h	C	0	0	0	1	0	1	0	0	0	Display off
DISPON	29h	2900h	C	0	0	0	1	0	1	0	0	1	Display on

Instruction	Address		R/W/C	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Function
	MIPI	SPI-16											
TEOFF	34h	3400h	C	0	0	0	1	1	0	1	0	0	Tearing effect line off
TEON	35h	3500h	W	0	0	0	1	1	0	1	0	1	Tearing effect line on
MADCTL	36h	3600h	W	1	--	--	--	ML	BGR	--	--	--	Display data access control
IDMOFF	38h	3800h	C	0	--	--	--	--	--	--	--	--	Idle mode off
IDMON	39h	3900h	C	0	--	--	--	--	--	--	--	--	Idle mode on
COLMOD	3Ah	3A00h	W	0	--	VIPF[2:0]			--	--	--	--	Interface Pixel Format
GSL	45h	4500h	R	2	TESL[15:8]								Read Tear line
		4501h			TESL[7:0]								
WRDIBV	51h	5100h	W	1	DBV[7:0]								Write display brightness
RDDISBV	52h	5200h	R	1	DBV[7:0]								Read display brightness value
WRCTRLD	53h	5300h	W	1	--	--	BCTRL	--	DD	BL	--	--	Write control display
RRCTRLD	54h	5400h	R	1	--	--	BCTRL	--	DD	BL	--	--	Read control display value
WRCABC	55h	5500h	W	1	CE_ON	--	CE_MD[1:0]		--	--	CABC_MD[1:0]		Write CABC mode
RRCABC	56h	5600h	R	1	CE_ON	--	CE_MD[1:0]		--	--	CABC_MD[1:0]		Read CABC mode
WRCABCMB	5Eh	5E00h	W	1	CMB[7:0]								Write CABC minimum brightness
RRCABCMB	5Fh	5F00h	R	1	CMB[7:0]								Read CABC minimum brightness
RDABCSD	68h	6800h	R	1	RLD	FUND	--	--	--	--	--	--	Read Automatic Brightness Control Self-Diagnostic Result
RDBWLB	70h	7000h	R	1	BKx1	BKx0	BKy1	BKy0	Wx1	Wx0	Wy1	Wy0	Read Black/White Low Bits
RDBkx	71h	7100h	R	1	BKx9	BKx8	BKx7	BKx6	BKx5	BKx4	BKx3	BKx2	Read BKx
RDBky	72h	7200h	R	1	BKy9	BKy8	BKy7	BKy6	BKy5	BKy4	BKy3	BKy2	Read Bky
RDWx	73h	7300h	R	1	Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx2	Read Wx
RDWy	74h	7400h	R	1	Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2	Read Wy
RDRGLB	75h	7500h	R	1	Rx1	Rx0	Ry1	Ry0	Gx1	Gx0	Gy1	Gy0	Read Red/Green Low bits
RDRx	76h	7600h	R	1	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	Read Rx
RDRy	77h	7700h	R	1	Ry9	Ry8	Ry7	Ry6	Ry5	Ry4	Ry3	Ry2	Read Ry
RDGx	78h	7800h	R	1	Gx9	Gx8	Gx7	Gx6	Gx5	Gx4	Gx3	Gx2	Read Gx
RDGy	79h	7900h	R	1	Gy9	Gy8	Gy7	Gy6	Gy5	Gy4	Gy3	Gy2	Read Gy
RDBALB	7Ah	7A00h	R	1	Bx1	Bx0	By1	By0	Ax1	Ax0	Ay1	Ay0	Blue/AColour Low Bits
RDBx	7Bh	7B00h	R	1	Bx9	Bx8	Bx7	Bx6	Bx5	Bx4	Bx3	Bx2	Read Bx
RDBy	7Ch	7C00h	R	1	By9	By8	By7	By6	By5	By4	By3	By2	Read By
RDAx	7Dh	7D00h	R	1	Ax9	Ax8	Ax7	Ax6	Ax5	Ax4	Ax3	Ax2	Read Ax
RDAy	7Eh	7E00h	R	1	Ay9	Ay8	Ay7	Ay6	Ay5	Ay4	At3	Ay2	Read Ay

Instruction	Address		R/W/C	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Function
	MIPI	SPI-16											
RDDDBS/ CHKSUM	A1h	A100h	R	5	0x88								Read the DDB from the provided location
		A101h			0x02								
		A102h			MID[15:8]								
		A103h			MID[7:0]								
		A104h			8'hff								
RDDDBC	A8h	A800h	R	5	SID[15:8]								Continue reading the DDB from the last read location
		A801h			SID[7:0]								
		A802h			MID[15:8]								
		A803h			MID[7:0]								
		A804h			8'hff								
RDFCS	AAh	AA00h	R	1	FCS[7:0]								Read First Checksum
RDCCS	AFh	AF00h	R	1	CCS[7:0]								Read Continue Checksum
RDID1	DAh	DA00h	R	1	ID1[7:0]								Read ID1
RDID2	DBh	DB00h	R	1	ID2[7:0]								Read ID2
RDID3	DCh	DC00h	R	1	ID3[7:0]								Read ID3

Table 24 System Function Command List

Note:

1. In MIPI interface, parameters of the command are stores onto registers when the last parameter of the command has been received. Also, parameters of the command are not stored onto registers if there has been happen a break. This note is valid when a number of the parameters is equal or less than 32.

2. The 8-bit address code for "MIPI" in above table and following command description means include 3-wire 9-bit SPI and 4-wire 8-bit SPI.

12.2.1 NOP (00/0000h)

<table>
<tr><td>00H</td><td colspan="12">NOP (No Operation)</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>NOP</td><td>W</td><td>00h</td><td>0000h</td><td colspan="9">No Argument</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command is empty command. It does not have effect on the display module.
However it can be used to terminate parameter write commands.</td></tr>
<tr><td>Restriction</td><td colspan="12"></td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"></td></tr>
</table>

12.2.2 SWRESET (01h/0100h): Software Reset

01H	SWRESET (Software Reset)											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
SWRESET	W	01h	0100h	xx	0	0	0	0	0	0	0	1
Parameter	No Parameter											
Description	"-" Don't care -The display module performs a software reset, registers are written with their SW reset default values. -Frame memory contents are unaffected by this command.											
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during this 5msec. If software reset is sent during sleep in mode, it will be necessary to wait 120msec before sending sleep out command. Software reset command cannot be sent during sleep out sequence. When MIPI Video Mode application, the shut down packet should be sent (leave to video mode) before S/W reset											

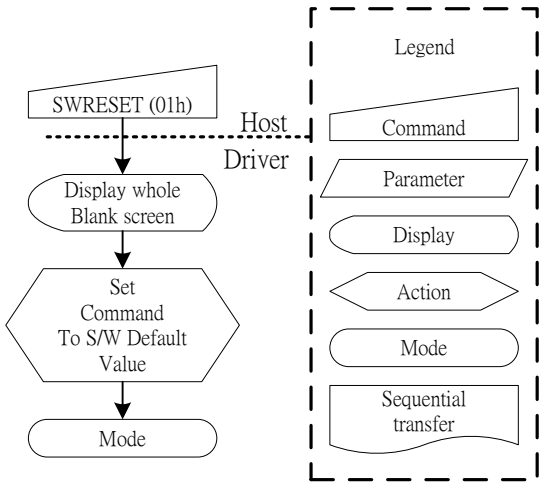
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

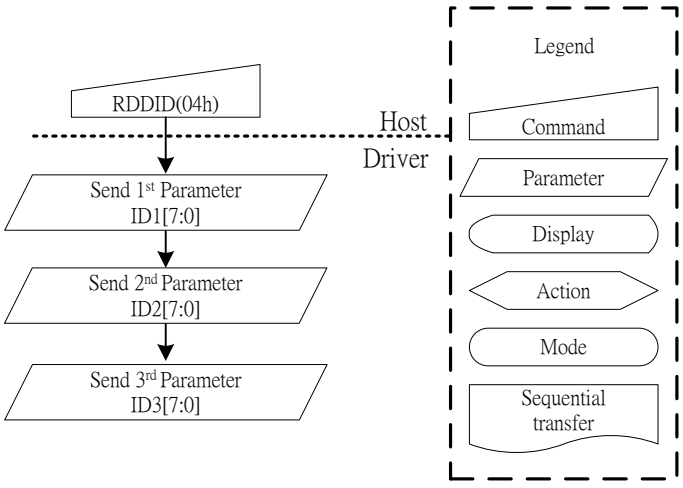
Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart



12.2.3 RDDID (04h/0400h~0402h): Read Display ID

<table>
<tr><td>04H</td><td colspan="12">RDDID (Read Display ID)</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td rowspan="3">RDDID</td><td rowspan="3">R</td><td rowspan="3">04h</td><td>0400h</td><td>00h</td><td colspan="8">ID1[7:0]</td></tr>
<tr><td>0401h</td><td>00h</td><td colspan="8">ID2[7:0]</td></tr>
<tr><td>0402h</td><td>00h</td><td colspan="8">ID3[7:0]</td></tr>
<tr><td>Description</td><td colspan="12">-This read byte returns 24-bit display identification information.
-The 1st parameter is dummy data
-The 2nd parameter (ID1): LCD module's manufacturer ID.
-The 3rd parameter (ID2): LCD module/driver version ID
-The 4th parameter (ID3): LCD module/driver ID.
-Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively.</td></tr>
<tr><td>Restriction</td><td colspan="12">-</td></tr>
<tr><td>Register availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>ID1</th><th>ID2</th><th>ID3</th></tr><tr><td>Power On Sequence</td><td>0xFF</td><td>0xFF</td><td>0xFF</td></tr><tr><td>S/W Reset</td><td>0xFF</td><td>0xFF</td><td>0xFF</td></tr><tr><td>H/W Reset</td><td>0xFF</td><td>0xFF</td><td>0xFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

12.2.4 RDNUMED (05h/0500h): Read Number of Errors on DSI

05H	RDNUMED										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		Others	SPI-16								
RDNUMED	R	05h	X	X	Errover	Err[6:0]						
Description	The first parameter is telling a number of the parity errors on DSI. The more detailed description of the bits is below. Err[6:0] bits are telling a number of the parity errors. Errover is set to “1” if there is overflow with P[6..0] bits. This command is used for MIPI DSI only. It is no function for others interface operation.											
Restriction	-											

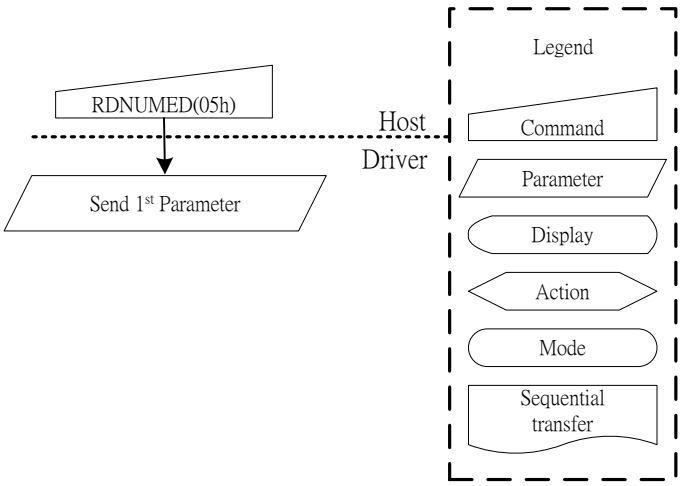
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	Errover	Err[6:0]
Power On Sequence	0	000-0000
S/W Reset	0	000-0000
H/W Reset	0	000-0000

Flow Chart



12.2.5 RDRED (06h/0600h): Read the first pixel of Red Color

06H	RDRED										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
RDRED	R	X	0600h	X	R_1st[7:0]							
Description	This command returns the red component value of the first pixel in the active frame. Only the relevant bits are used according to pixel format, unused bits are set to “0”. -16-bit format: R4 is MSB and R0 is LSB. R7, R6 and R5 are set to “0”. -18-bit format: R5 is MSB and R0 is LSB. R7 and R6 are set to “0”. -24-bit format: R7 is MSB and R0 is LSB.											
Restriction	-											

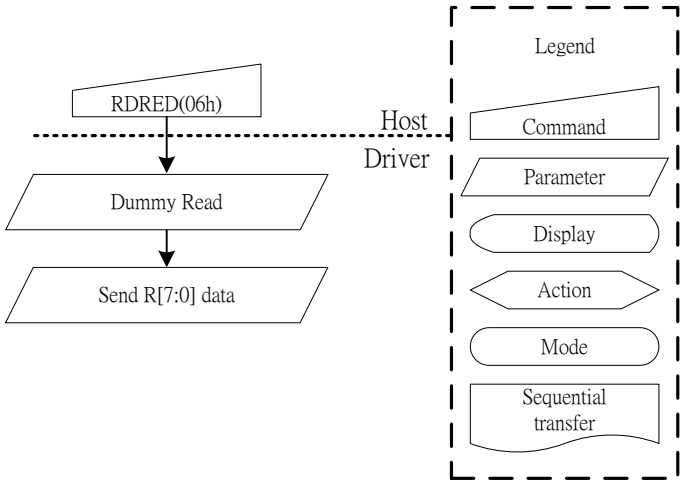
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



12.2.6 RDGREEN (07h/0700h): Read the first pixel of Green Color

07H	RDGREEN										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
RDGREEN	R	X	0700h	X	G_1st[7:0]							
Description	This command returns the green component value of the first pixel in the active frame. Only the relevant bits are used according to pixel format, unused bits are set to “0”. -16-bit format: G4 is MSB and G0 is LSB. G7, G6 and G5 are set to “0”. -18-bit format: G5 is MSB and G0 is LSB. G7 and G6 are set to “0”. -24-bit format: G7 is MSB and G0 is LSB.											
Restriction	-											

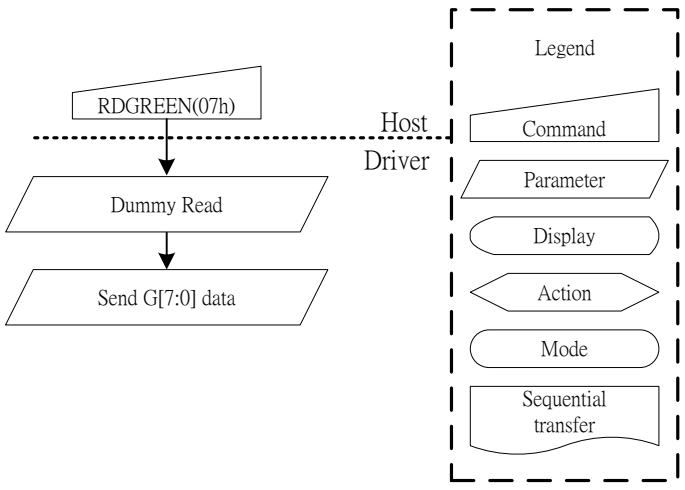
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



12.2.7 RDBLUE (08h/0800h): Read the first pixel of Blue Color

08H	RDBLUE											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
RDBLUE	R	X	0800h	X	B_1st[7:0]							
Description	This command returns the blue component value of the first pixel in the active frame. Only the relevant bits are used according to pixel format, unused bits are set to “0”. -16-bit format: B4 is MSB and B0 is LSB. B7, B6 and B5 are set to “0”. -18-bit format: B5 is MSB and B0 is LSB. B7 and B6 are set to “0”. -24-bit format: B7 is MSB and B0 is LSB.											
Restriction	-											

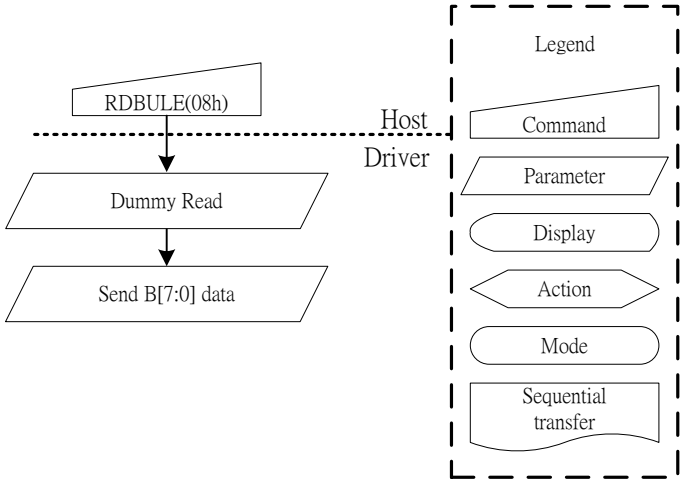
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



12.2.8 RDDPM (0Ah/0A00h): Read Display Power Mode

0AH	RDDPM										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
RDDPM	R	0Ah	0A00h	X	BSTON	0	0	SLPOUT	1	DISON	--	--

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Booster Voltage Status	"1"=Booster On, "0"=Booster Off
D6	Not Defined	Set to "0" (not used)
D5	Not Defined	Set to "0" (not used)
D4	Sleep In/Out	"1" = Sleep Out Mode, "0" = Sleep In Mode
D3	Not Defined	Set to "1" (not used)
D2	Display On/Off	"1" = Display is On, "0" = Display is Off
D1	Not Defined	Set to "0" (not used)
D0	Not Defined	Set to "0" (not used)

Restriction

-

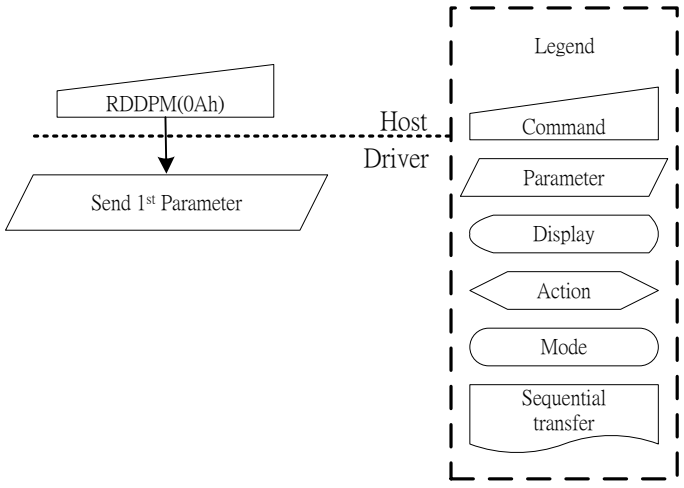
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

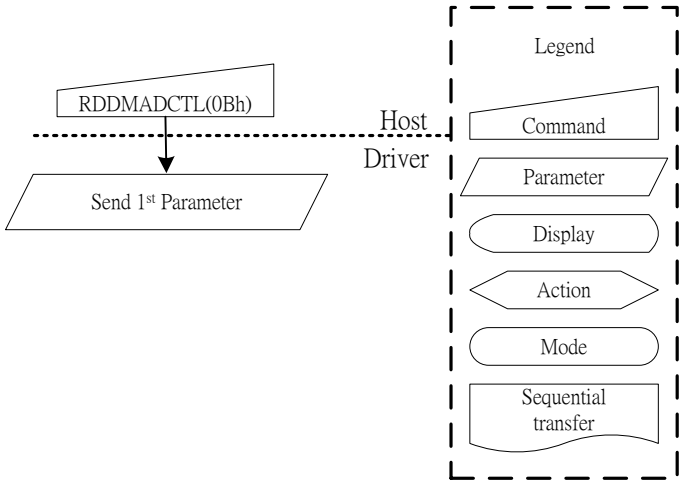
Default

Status	Default Value (D7 to D0)
Power On Sequence	08h
S/W Reset	08h
H/W Reset	08h

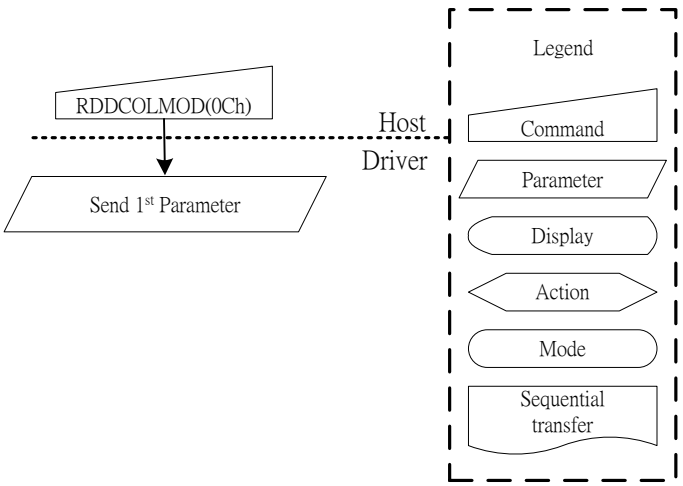
Flow Chart



12.2.9 RDDMADCTL (0Bh/0B00h): Read Display MADCTL

<table>
<tr><td>0BH</td><td colspan="12">RDDMADCTL</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>RDDMADCTL</td><td>R</td><td>0Bh</td><td>0B00h</td><td>X</td><td>--</td><td>--</td><td>--</td><td>ML</td><td>BGR</td><td>--</td><td>--</td><td>--</td></tr>
<tr><td>Description</td><td colspan="12">This command indicates the current status of the display as described in the table below:
<table>
<tr><td>Bit</td><td>Description</td><td>Value</td></tr>
<tr><td>D7~D5</td><td>Not Defined</td><td>Set to “0” (not used)</td></tr>
<tr><td>D4</td><td>Vertical refresh Order (ML)</td><td>“0” = Increment , “1” = Decrement</td></tr>
<tr><td>D3</td><td>RGB-BGR Order</td><td>“0” = RGB color sequence
“1” = BGR color sequence</td></tr>
<tr><td>D2</td><td>--</td><td>“0”</td></tr>
<tr><td>D1</td><td>Not Defined</td><td>Set to “0” (not used)</td></tr>
<tr><td>D0</td><td>Not Defined</td><td>Set to “0” (not used)</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">-</td></tr>
<tr><td>Register availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value (D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

12.2.10 RDDCOLMOD (0Ch/0C00h): Read Display Pixel Format

<table>
<tr><td>0CH</td><td colspan="12">RDDCOLMOD</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>RDDCOLMOD</td><td>R</td><td>0Ch</td><td>0C00h</td><td>X</td><td>--</td><td colspan="3">VIPF[2:0]</td><td>--</td><td>--</td><td>--</td><td>--</td></tr>
<tr><td>Description</td><td colspan="12">This command indicates the current status of the display as described in the table below:
<table>
<tr><td>Bit</td><td>Description</td><td>Value</td></tr>
<tr><td>D7</td><td>Not Defined</td><td>Set to “0” (not used)</td></tr>
<tr><td>D6~D4</td><td>RGB Interface Color Format</td><td>“101” = 16-bit / pixel
“110” = 18-bit / pixel
“111” = 24-bit / pixel</td></tr>
<tr><td>D3</td><td>Not Defined</td><td>Set to “0” (not used)</td></tr>
<tr><td>D2</td><td>Not Defined</td><td>Set to “0” (not used)</td></tr>
<tr><td>D1</td><td>Not Defined</td><td>Set to “0” (not used)</td></tr>
<tr><td>D0</td><td>Not Defined</td><td>Set to “0” (not used)</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">-</td></tr>
<tr><td>Register availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value (D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>70h</td></tr>
<tr><td>S/W Reset</td><td>70h</td></tr>
<tr><td>H/W Reset</td><td>70h</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

12.2.11 RDDIM (0Dh/0D00h): Read Display Image Mode

0DH	RDDIM											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
RDDIM	R	0Dh	0D00h	X	--	--	INVON	ALPXLON	ALPXLOFF	GCS[2:0]		

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7~D6	Not Defined	Set to “00” (not used)
D5	Inversion On/Off	“1”=Inversion On, “0”=Inversion Off
D4	All Pixel On	“1”=White display,”0”=Normal display
D3	All Pixel Off	“1”=Black display,“0”=Normal display
D2~D0	Gamma Curve Selection	“000”=GC0, “001”=GC1 “010”=GC2, “011”=GC3 “110” to “111”=not defined

Restriction

-

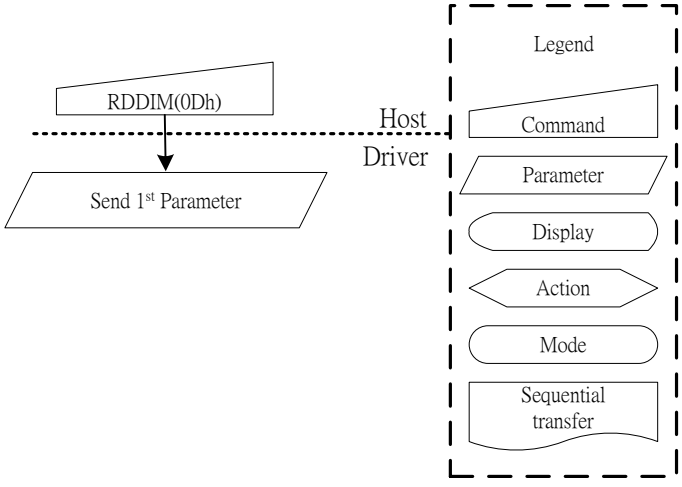
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



12.2.12 RDDSM (0Eh/0E00h): Read Display Signal Mode

0EH	RDDSM											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
RDDSM	R	0Eh	0E00h	X	TEON	TELMD	--	--	--	--	--	--

Description

Bit	Description	Value
D7	Tearing Effect Line On/Off	"1"=On,"0"=Off
D6	Tearing Effect Line Mode	"1"=Mode2,"0"=Mode1
D4~D0	Not Defined	Set to "00000" (not used)

Restriction

-

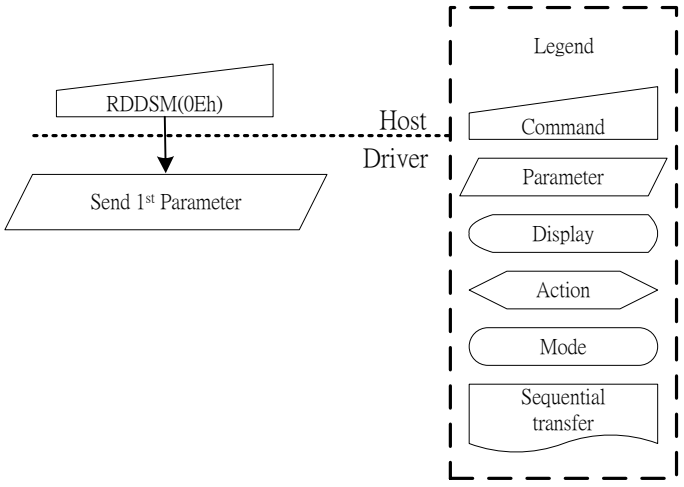
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



12.2.13 RDDSDR (0Fh/0F00h): Read Display Self-Diagnostic Result

0FH	RDDSDR										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
RDDSDR	R	0Fh	0F00h	X	RLD	FUND	0	0	--	--	--	--

Description

Bit	Description	Value
D7	Register Loading Detection	See section 10.3.1
D5	Functionality Detection	See section 10.3.2
D5~D0	Not Defined	Set to “000000” (not used)

Restriction

-

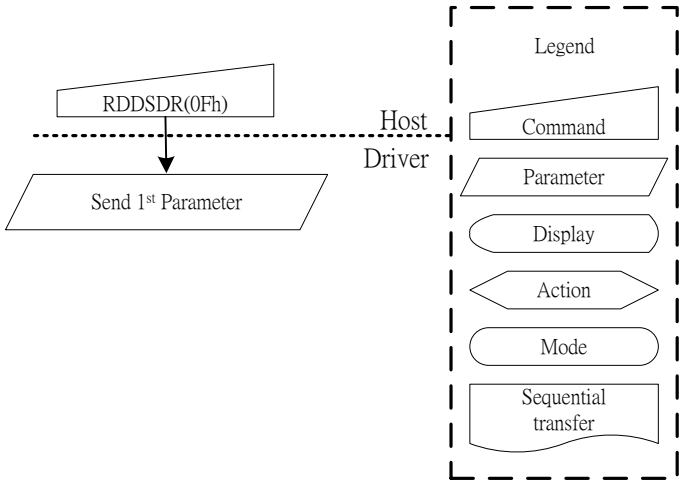
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



12.2.14 SLPIN (10h/1000h): Sleep in

10H	SLPIN											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
SLPIN	W	10h	1000h	X	No Argument							

Description

This command causes the TFT LCD module to enter the minimum power consumption mode.
In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.
Control Interface as will as display data and registers are still working.
User can send PCLK, HS and VS information on RGB I/F for blank display after Sleep In command and this information is valid during 2 frames after Sleep In command if there is used Normal Mode On in Sleep Out-mode.
Dimming function does not work when there is changing mode from Sleep Out to Sleep In.
There is used an internal oscillator for blank display

Restriction

-

Register availability

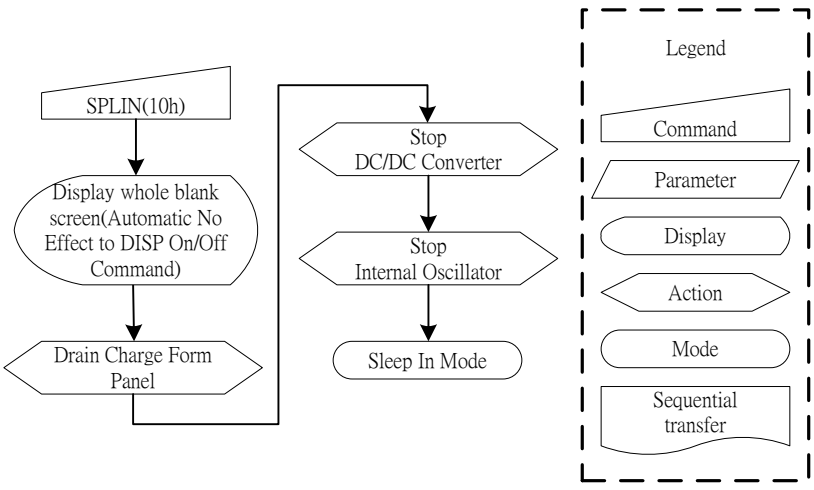
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

Flow Chart

It takes about 120 msec to get into Sleep In mode (booster off state) after SLPIN command issued.
The results of booster off can be check by RDDST (0Ah) command D7.



12.2.15 SLPOUT (11h/1100h): Sleep Out

11H	SLPOUT											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
SLPOUT	W	11h	1100h	X	No Argument							
Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started. User can start to send PCLK, HS and VS information on RGB I/F before Sleep Out command and this information is valid at least 2 frames before Sleep Out command, if there is left Sleep In-mode to Sleep Out-mode in Normal Mode On. There is used an internal oscillator for blank display. ST7701S will do sequence control about gate control signals when sleep out.											
Restriction	-											

Register availability

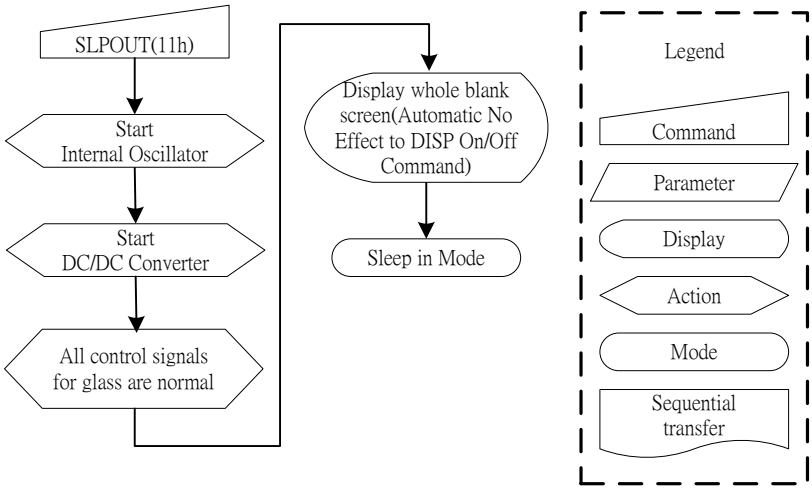
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

Flow Chart

It takes about 120 msec to get into Sleep In mode (booster off state) after SLPIN command issued.



12.2.16 PTLON (12h/1200h): Partial Display Mode On

<table>
<tr><td>12H</td><td colspan="11">PTLON</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>PTLON</td><td>W</td><td>12h</td><td>1200h</td><td>X</td><td colspan="7">No Argument</td></tr>
<tr><td>Description</td><td colspan="11">This command turns on Partial mode. The partial mode window is described by the Partial Area command .
To leave Partial mode, the Normal Display Mode On command (13H) should be written.
There is no abnormal visual effect during mode change between Normal mode On to Partial mode On.</td></tr>
<tr><td>Restriction</td><td colspan="11">This command has no effect when Partial Display mode is active.</td></tr>
<tr><td>Register availability</td><td colspan="11"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="11"><table><tr><th>Status</th><th>Default Value (D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>Normal Mode On</td></tr><tr><td>S/W Reset</td><td>Normal Mode On</td></tr><tr><td>H/W Reset</td><td>Normal Mode On</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="11">See Partial Area (30h)</td></tr>
</table>

12.2.17 NORON (13h/1300h): Normal Display Mode On

13H	NORON										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
NORON	W	13h	1300h	X	No Argument							
Description	This command returns the display to normal mode. Normal display mode on means Partial mode off. Exit from NORON by the Partial mode On command (12h) There is no abnormal visual effect during mode change from Partial mode On to Normal mode On.											
Restriction	This command has no effect when Normal Display mode is active.											

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	Normal Mode On
S/W Reset	Normal Mode On
H/W Reset	Normal Mode On

Flow Chart: See Partial Area Definition Descriptions for details of when to use this command

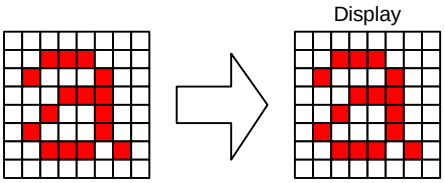
12.2.18 INVOFF (20h/2000h): Display Inversion Off

20H	INVOFF											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
INVOFF	W	20h	2000h	X	No Argument							

Description

This command is used to recover from display inversion mode.

This command does not change any other status.



Restriction

This command has no effect when module is already in Inversion Off mode.

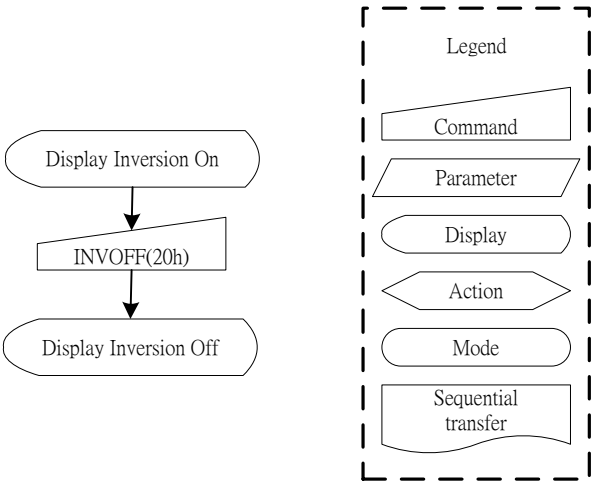
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

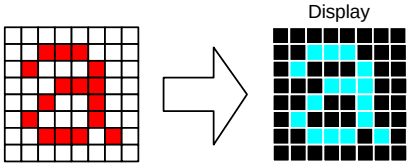
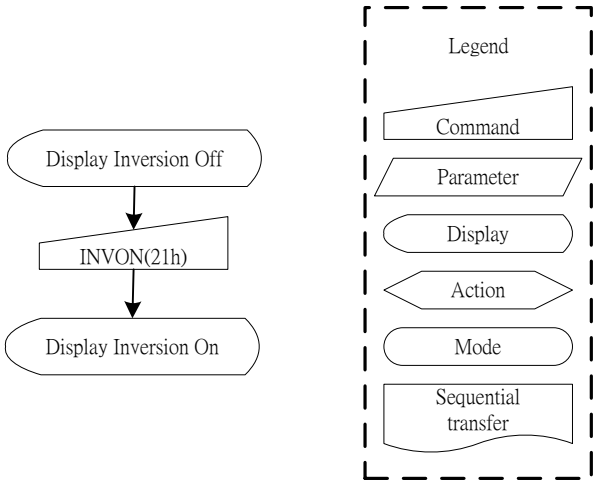
Default

Status	Default Value (D7 to D0)
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

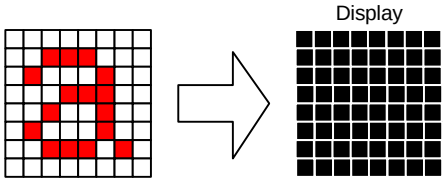
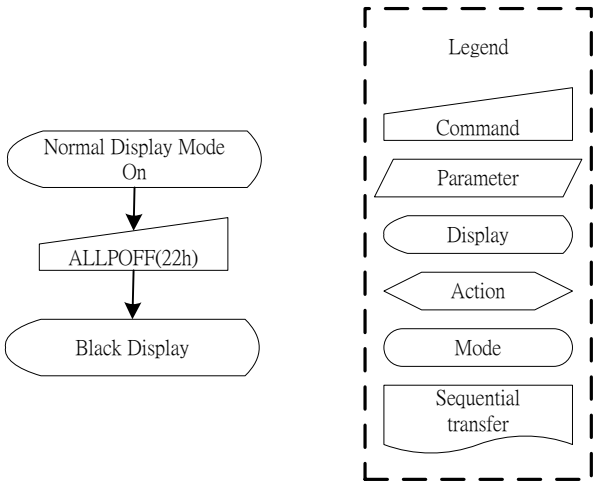
Flow Chart



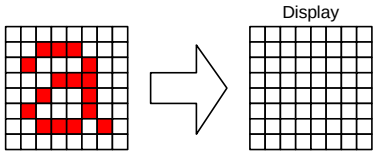
12.2.19 INVON (21h/2100h): Display Inversion On

<table>
<tr><td>21H</td><td colspan="12">INVON</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>INVON</td><td>W</td><td>21h</td><td>2100h</td><td>X</td><td colspan="8">No Argument</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to enter display inversion mode.
This command does not change any other status.
To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.
  </td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when module is already in Inversion On mode.</td></tr>
<tr><td>Register availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value (D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>Display Inversion off</td></tr><tr><td>S/W Reset</td><td>Display Inversion off</td></tr><tr><td>H/W Reset</td><td>Display Inversion off</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12">  </td></tr>
</table>

12.2.20 ALLPOFF (22h/2200h): All Pixel Off

<table>
<tr><td>22H</td><td colspan="11">ALLPOFF</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>ALLPOFF</td><td>W</td><td>22h</td><td>2200h</td><td>X</td><td colspan="7">No Argument</td></tr>
<tr><td>Description</td><td colspan="11">This command turns the display panel black in Sleep Out mode and a status of the Display On/Off register can be on or off. This command does not change any other status.
  </td></tr>
<tr><td>Restriction</td><td colspan="11">This command has no effect when module is already in All Pixel Off mode.</td></tr>
<tr><td>Register availability</td><td colspan="11"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="11"><table><tr><th>Status</th><th>Default Value (D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>All pixel off</td></tr><tr><td>S/W Reset</td><td>All pixel off</td></tr><tr><td>H/W Reset</td><td>All pixel off</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="11">  </td></tr>
</table>

12.2.21 ALLPON (23h/2300h): All Pixel ON

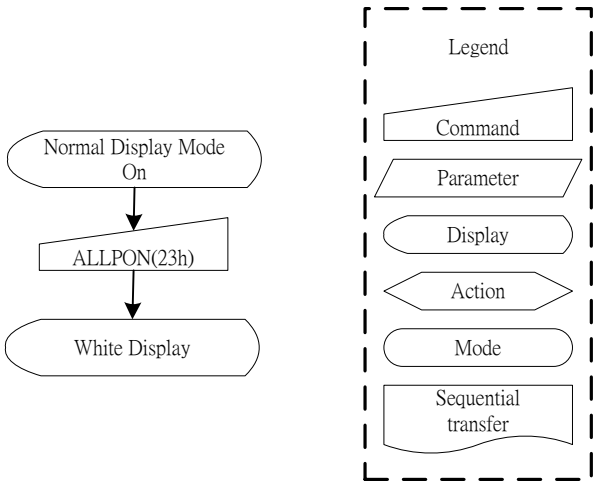
23H	ALLPON										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
ALLPOFF	W	23h	2300h	X	No Argument							
Description	This command turns the display panel white in Sleep Out mode and a status of the Display On/Off register can be on or off.This command does not change any other status.  “All Pixels Off” or “Normal Display Mode On” commands are used to leave this mode. The display panel is showing the display data after “Normal Display On” command.										
Restriction	This command has no effect when module is already in all Pixel On mode.										
Register availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

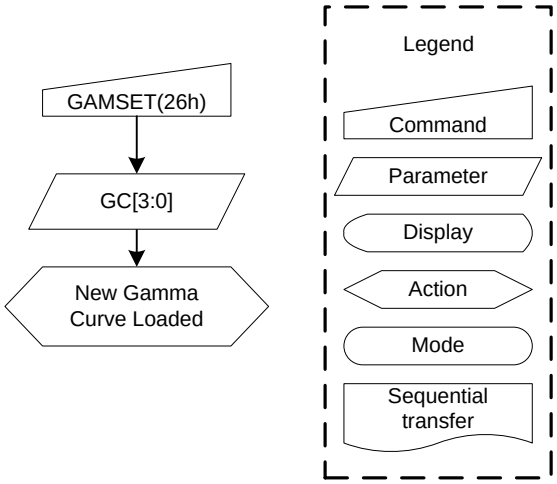
Default

Status	Default Value (D7 to D0)
Power On Sequence	All Pixel off
S/W Reset	All Pixel off
H/W Reset	All Pixel off

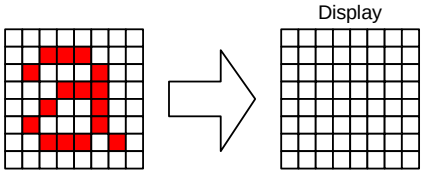
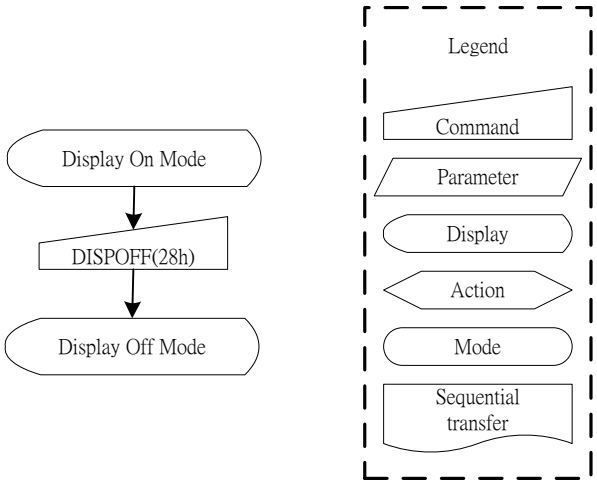
Flow Chart



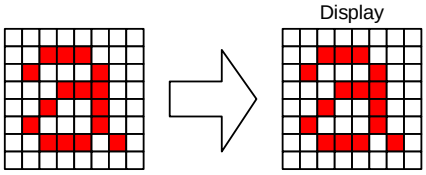
12.2.22 GAMSET (26h/2600h): Gamma Set

<table>
<tr><td>26H</td><td colspan="11">GAMSET</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>GAMSET</td><td>W</td><td>23h</td><td>2300h</td><td>X</td><td>--</td><td>--</td><td>--</td><td>--</td><td colspan="5">GC[3:0]</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table.
<table>
<tr><th>GC[3:0]</th><th>Parameter</th><th>Curve Selected</th></tr>
<tr><td>01h</td><td>GC0</td><td>Gamma Curve 1 (G=2.2)</td></tr>
<tr><td>02h</td><td>GC1</td><td>Reserved</td></tr>
<tr><td>04h</td><td>GC2</td><td>Reserved</td></tr>
<tr><td>08h</td><td>GC3</td><td>Reserved</td></tr>
</table>
Note :All other values are undefined.</td></tr>
<tr><td>Restriction</td><td colspan="12">Values of GC [7:0] not shown in table above are invalid and will not change the current selected gamma curve until valid is received.</td></tr>
<tr><td>Register availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value (D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>Reserved</td></tr>
<tr><td>S/W Reset</td><td>Reserved</td></tr>
<tr><td>H/W Reset</td><td>Reserved</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

12.2.23 DISPOFF (28h/2800h): Display Off

<table>
<tr><td>28H</td><td colspan="12">DISPOFF</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>DISPOFF</td><td>W</td><td>28h</td><td>2800h</td><td>X</td><td colspan="8">No Argument</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to enter into DISPLAY OFF mode. In this mode, the display data is disables and blank page inserted.
This command does not change any other status. There will be no abnormal visible effect on the display.
  </td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when module is already in Display Off mode.</td></tr>
<tr><td>Register availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value (D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>Display off</td></tr><tr><td>S/W Reset</td><td>Display off</td></tr><tr><td>H/W Reset</td><td>Display off</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12">  </td></tr>
</table>

12.2.24 DISPON (29h/2900h): Display On

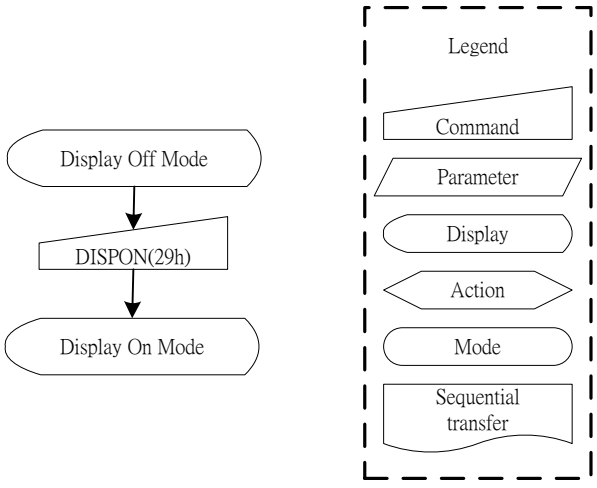
29H	DISPON										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
DISPON	W	29h	2900h	X	No Argument							
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the display data is disables and blank page inserted. This command does not change any other status. There will be no abnormal visible effect on the display. 											
Restriction	This command has no effect when module is already in Display Off mode.											
Register availability												

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



12.2.25 TEOFF (34h/3400h):Tearing Effect Line OFF

34H	TEOFF											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
TEOFF	W	34h	3400h	X	No Argument							
Description	This command is used to turn off the Display module's Tearing Effect output signal (Active Low) on the TE signal line.											
Restriction	This command has no effect when the Tearing Effect output is already OFF.											

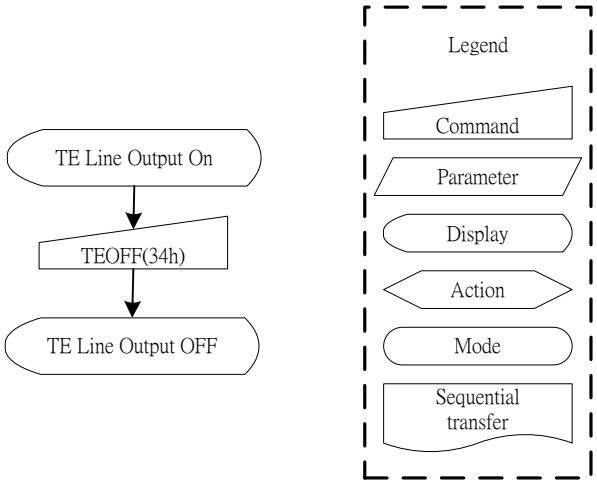
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



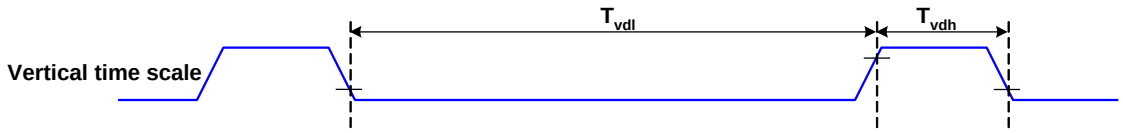
12.2.26 TEON (35h/3500h):Tearing Effect Line ON

35H	TEON										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
TEOFF	W	35h	3500h	X	--	--	--	--	--	--	--	M

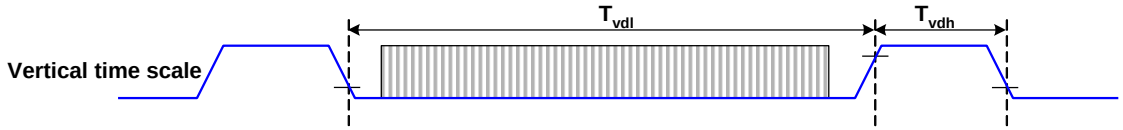
Description

This command is used to turn ON the Tearing Effect output signal on the TE signal line. Changing the MADCTL bit B4 will not affect this output. The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line.

When M = 0: The Tearing Effect Output line consists of V-Blanking information only:



When M = 1: The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:



Note: During the Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

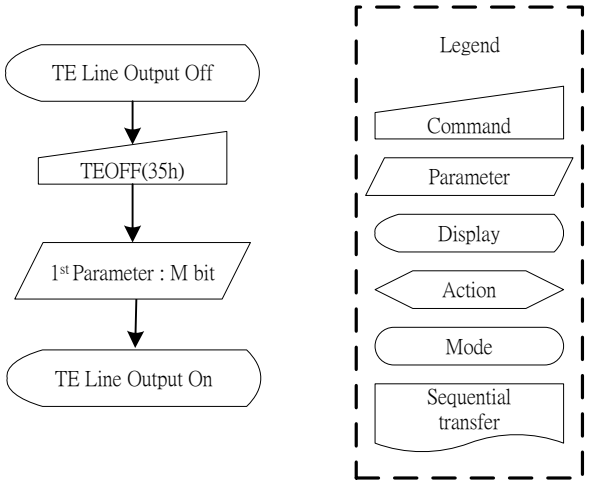
This command has no effect when the Tearing Effect output is already OFF.

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart	

12.2.27 MADCTL(36h/3600h): Display data access control

36H	IDMOFF										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
IDMOFF	W	36h	3600h	X	--	--	--	ML	BGR	--	--	--
Description	**ML**: GET Scan direction selection. ML= 0 Get normal scan. ML=1 Get reverse scan. **BGR**: BGR=0 ➔RGB BGR=1 ➔BGR											
Restriction	This command has no effect when module is already in Idle Off mode.											

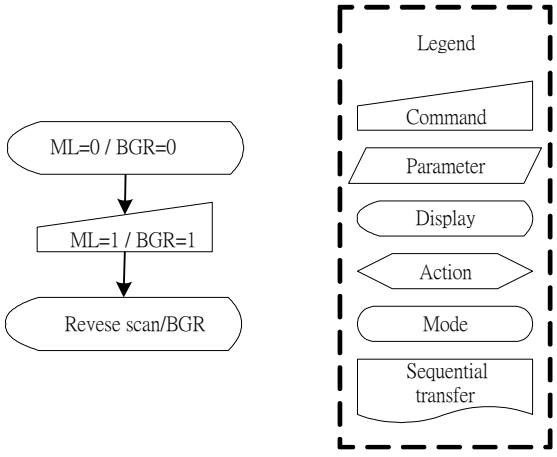
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00H
S/W Reset	00H
H/W Reset	00H

Flow Chart



12.2.28 IDMOFF (38h/3800h): Idle Mode Off

38H	IDMOFF											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
IDMOFF	W	38h	3800h	X	No Argument							
Description	This command is used to recover from Idle mode on In the idle off mode, display panel can display maximum 16.7M colors.											
Restriction	This command has no effect when module is already in Idle Off mode.											

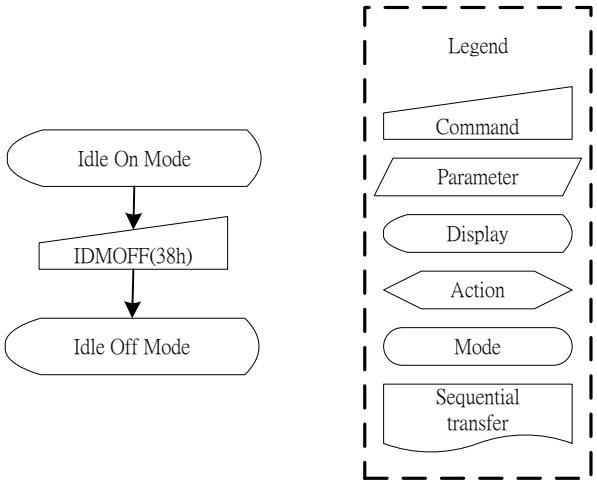
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	Idle Mode off
S/W Reset	Idle Mode off
H/W Reset	Idle Mode off

Flow Chart



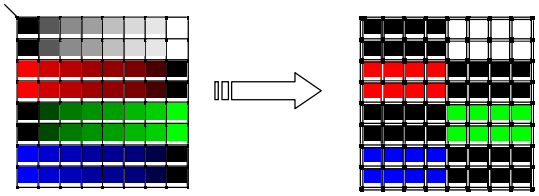
12.2.29 IDMON (39h/3900h): Idle Mode On

39H	IDMON											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
IDMON	W	39h	3900h	X	No Argument							

Description

(Example)Frame Data Display

Top-Left (0,0)



This command is used to enter into Idle mode on.

In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G, and B in Frame Data, 8 color depth data is displayed.

Color	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B4 B1 B0
Black	0xxxxx	0xxxxx	0xxxxx
Blue	0xxxxx	0xxxxx	1xxxxx
Red	1xxxxx	0xxxxx	0xxxxx
Magenta	1xxxxx	0xxxxx	1xxxxx
Green	0xxxxx	1xxxxx	0xxxxx
Cyan	0xxxxx	1xxxxx	1xxxxx
Yellow	1xxxxx	1xxxxx	0xxxxx
White	1xxxxx	1xxxxx	1xxxxx

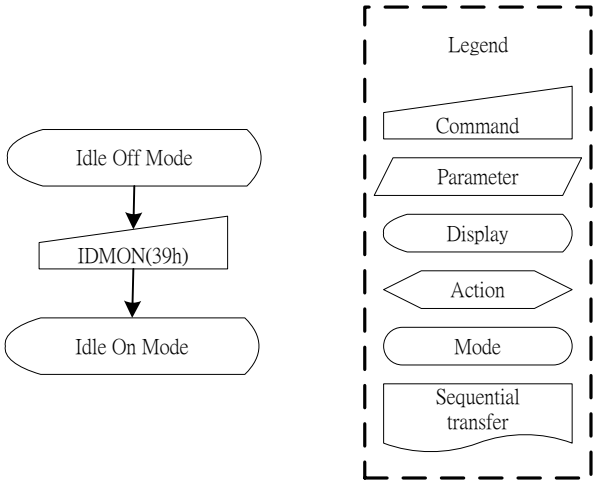
Restriction: This command has no effect when module is already in Idle On mode.

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	Idle Mode off
S/W Reset	Idle Mode off
H/W Reset	Idle Mode off

Flow Chart	

12.2.30 COLMOD (3Ah/3A00h): Interface Pixel Format

3AH	COLMOD										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
COLMOD	W	3Ah	3A00h	X	--	VIPF[2:0]			--	--	--	--

Description

This command is used to define the format of RGB picture data.

The formats are shown in the table:

Bit	NAME	DESCRIPTION
VIPF[2:0]	Pixel Format for RGB Interface	"101"=16-bit/pixel "110"=18-bit/pixel "111"=24-bit/pixel The others=not defined

Restriction

There is no visible effect until the display data is written to.

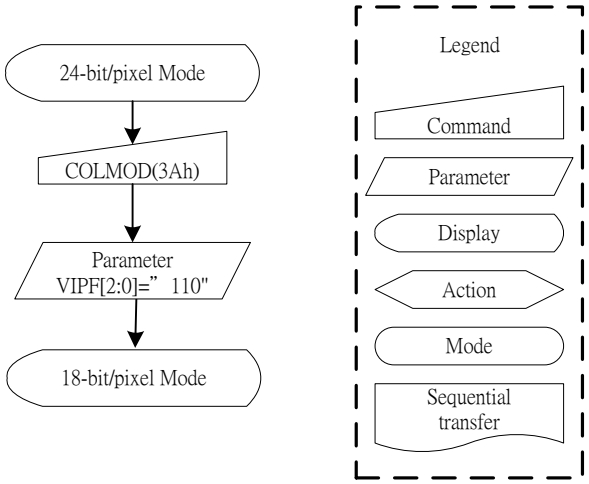
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	70h
S/W Reset	70h
H/W Reset	70h

Flow Chart



12.2.31 GSL (45h): Get Scan Line

45H	GSL											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
GSL	R	45h	4500h	X	TELS[15:8]							
			4501h	X	TELS[7:0]							
Description	The display reads the current scan line N, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0.											
Restriction	--											

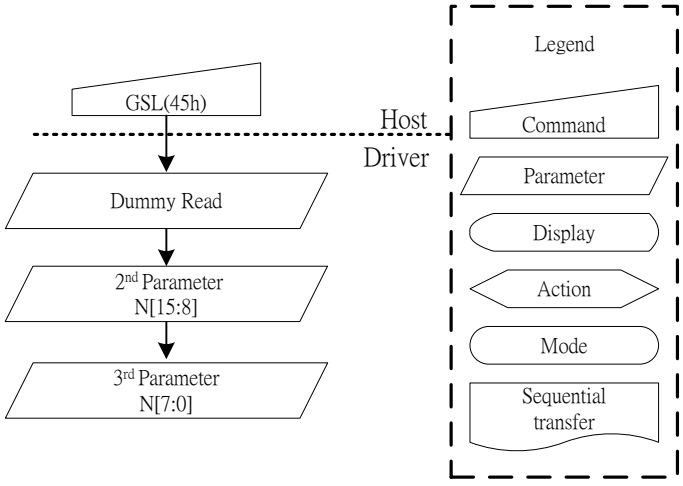
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



12.2.32 WRDISBV (51h): Write Display Brightness

51H	WRDISBV											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
WRDISBV	W	51h	5100h	X	DBV[7:0]							
Description	This command is used to adjust the brightness value of the display. It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display module specification. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.											
Restriction	The display supplier cannot use this command for tuning (e.g. factory tuning, etc.).											

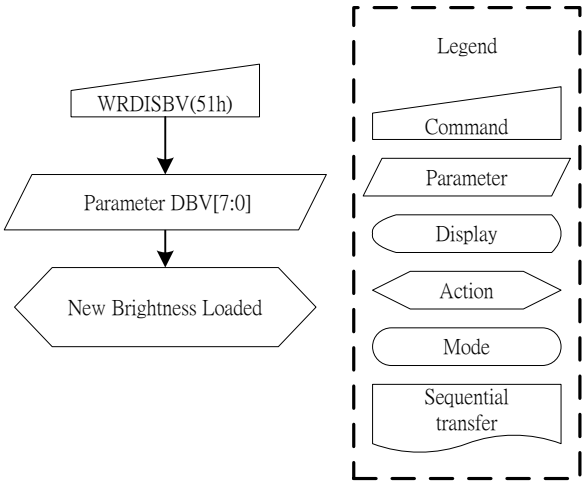
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



12.2.33 RDDISBV (52h/5200h): Read Display Brightness Value

52H	RDDISBV											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
WRDISBV	R	52h	5200h	X	DBV[7:0]							
Description	This command returns the brightness value of the display. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification is. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. DBV[7:0] is reset when display is in sleep in mode. DBV[7:0] is '0' when bit BCTRL of write CTRL display command (53h) is '0' DBV[7:0] IS manual set brightness specified with write CTRL display command (53h) when bit BCTRL is '1'											
Restriction	--											

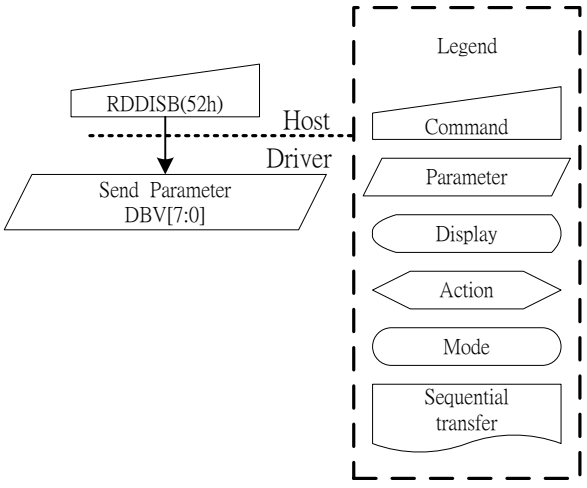
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

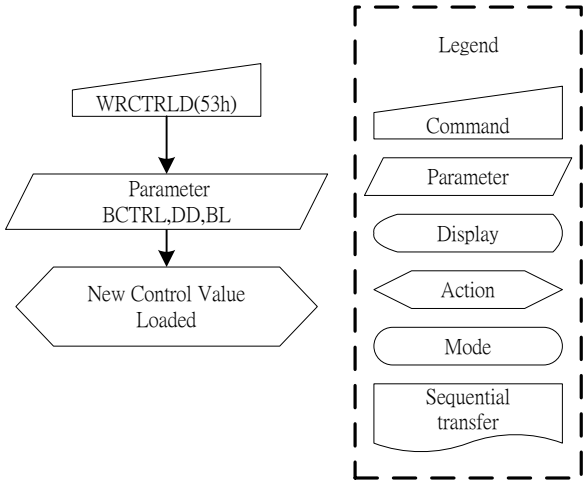
Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



12.2.34 WRCTRLD (53h/5300h): Write CTRL Display

<table>
<tr><td>53H</td><td colspan="12">WRCTRLD</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>WRCTRLD</td><td>W</td><td>53h</td><td>5300h</td><td>X</td><td>--</td><td>--</td><td>BCTRL</td><td>--</td><td>DD</td><td>BL</td><td>--</td><td>--</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to control display brightness.
BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.
0 = Off (Brightness register are 00h, DBV[7:0])
1 = On (Brightness register are active, according to the other parameters.)
DD: Display Dimming (Only for manual brightness setting)
DD = 0: Display Dimming is off.
DD = 1: Display Dimming is on.
BL: Backlight Control On/Off
0 = Off (Completely turn off backlight circuit. Control lines must be low.)
1 = On
Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1.
When BL bit changed from ‘on’ to ‘off’, backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.</td></tr>
<tr><td>Restriction</td><td colspan="12">--</td></tr>
<tr><td>Register availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value (D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table></td></tr>
</table>

Flow Chart	

12.2.35 RDCTRLD (54h): Read CTRL Value Display

54H	WRCTRLD										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
RDCTRLD	R	54h	5400h	X	--	--	BCTRL	--	DD	BL	--	--

Description

This command returns ambient light and brightness control values..

BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.

0 = Off 1 = On

DD: Display Dimming (Only for manual brightness setting)

DD = 0 DD = 1

BL: Backlight Control On/Off

0 = Off 1 = On

Restriction

--

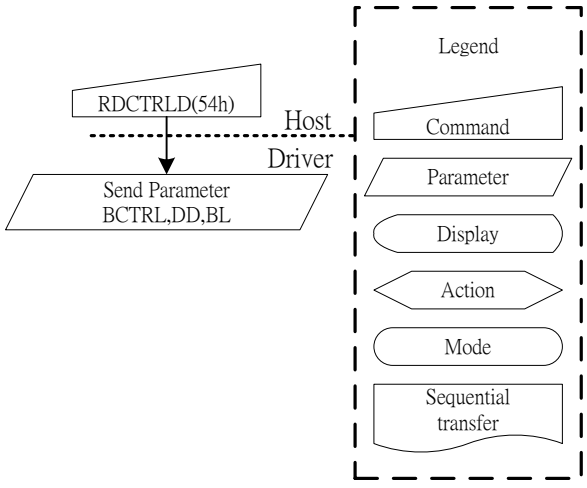
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

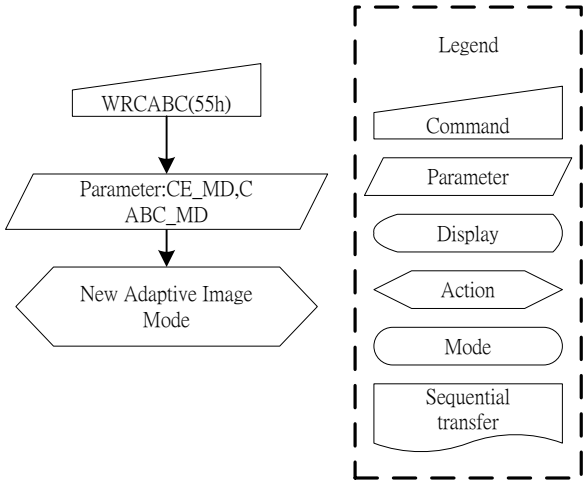
Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



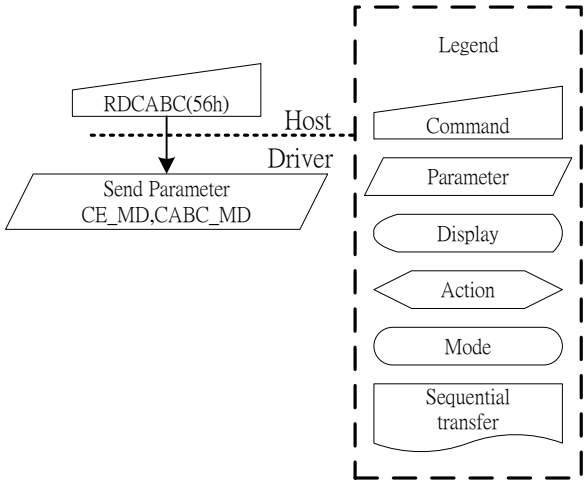
12.2.36 WRCACE (55h/5500h): Write Content Adaptive Brightness Control and Color Enhancement

<table>
<tr><td>55H</td><td colspan="12">WRCACE</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>WRCACE</td><td>W</td><td>55h</td><td>5500h</td><td>X</td><td>CE_ON</td><td>--</td><td colspan="2">CEMD[1:0]</td><td>--</td><td>--</td><td colspan="2">CABC_MD[1:0]</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to set parameters for image content based adaptive brightness control functionality and Color Enhancement function
CE_ON=”1”,Color enhancement on CE_ON=”0”,Color enhancement off
There are three color enhancement levels can be set.
<table>
<tr><th>CEMD[1]</th><th>CEMD[0]</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Low enhancement</td></tr>
<tr><td>0</td><td>1</td><td>Medium enhancement</td></tr>
<tr><td>1</td><td>1</td><td>High enhancement</td></tr>
</table>
There is possible to used 4 different modes for content adaptive image functionality, which are defined on a table below.
<table>
<tr><th>CABC_MD[1]</th><th>CABC_MD[0]</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Off</td></tr>
<tr><td>0</td><td>1</td><td>User Interface Mode</td></tr>
<tr><td>1</td><td>0</td><td>Still Picture</td></tr>
<tr><td>1</td><td>1</td><td>Moving Image</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">--</td></tr>
<tr><td>Register availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value (D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table></td></tr>
</table>

Flow Chart	

12.2.37 RDCABC (56h/5600h): Read Content Adaptive Brightness Control

<table>
<tr><td>56H</td><td colspan="12">RDCABC</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>RDCABC</td><td>R</td><td>56h</td><td>5600h</td><td>X</td><td>CE_ON</td><td>--</td><td colspan="2">CEMD[1:0]</td><td>--</td><td>--</td><td colspan="2">CABC_MD[1:0]</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to read the settings for image content based adaptive brightness control functionality.
CE_ON=”1”,Color enhancement on CE_ON=”0”,Color enhancement off
There are three color enhancement levels can be set.
<table>
<tr><th>CEMD[1]</th><th>CEMD[0]</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Low enhancement</td></tr>
<tr><td>0</td><td>1</td><td>Medium enhancement</td></tr>
<tr><td>1</td><td>1</td><td>High enhancement</td></tr>
</table>
There is possible to used 4 different modes for content adaptive image functionality, which are defined on a table below.
<table>
<tr><th>CABC_MD[1]</th><th>CABC_MD[0]</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Off</td></tr>
<tr><td>0</td><td>1</td><td>User Interface Mode</td></tr>
<tr><td>1</td><td>0</td><td>Still Picture</td></tr>
<tr><td>1</td><td>1</td><td>Moving Image</td></tr>
</table>
‘-’: Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="12">--</td></tr>
<tr><td>Register availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value (D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
</table>

Flow Chart	

12.2.38 WRCABCMB (5Eh/5E00h): Write CABC Minimum Brightness

5EH	WRCABCMB											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
WRCABCMB	W	5Eh	5E00h	X	CMB[7:0]							
Description	This command is used to set the minimum brightness value of the display for CABC function. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the brightness for CABC.											
Restriction	--											

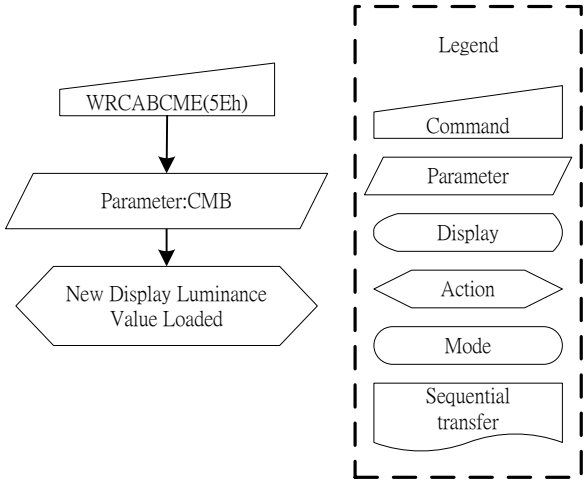
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



12.2.39 RDCABCMB (5Fh/5F00h): Read CABC Minimum Brightness

5FH	WRCABCMB											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
WRCABCMB	R	5Fh	5F00h	X	CMB[7:0]							
Description	This command returns the minimum brightness value of CABC function. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the brightness for CABC.											
Restriction	--											

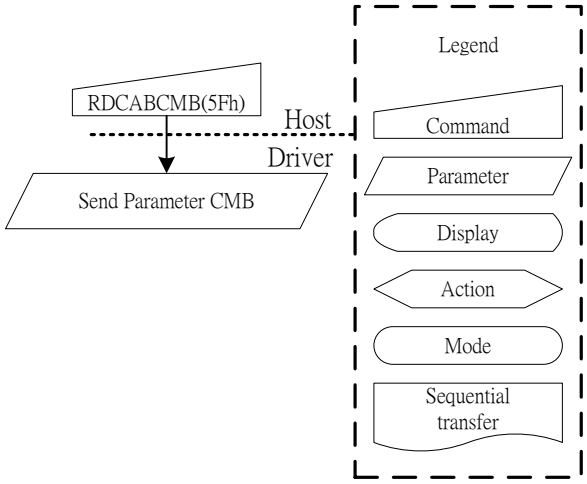
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



12.2.40 RDABCSDR (68h/6800h): Read Automatic Brightness Control Self-Diagnostic Result

68H	WRCABCMB											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
WRCABCMB	R	68h	6800h	X	RLD	FUND	--	--	--	--	--	--
Description	This command indicates the current status of the display self-diagnostic results for automatic brightness control after sleep out -command as described below: -RLD: Register loading detection -FUND: Functionality detection "-" Don't care											
Restriction	--											

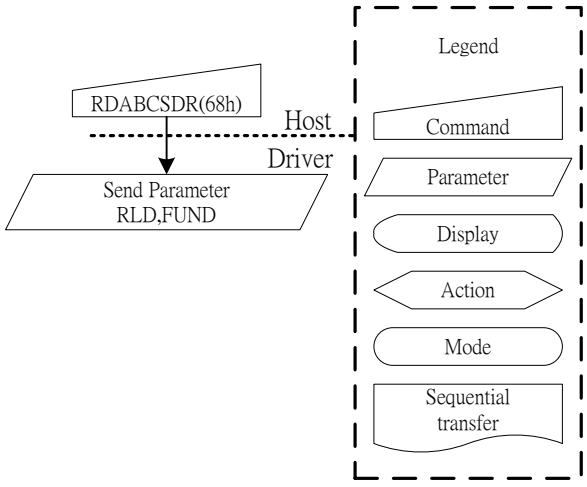
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



12.2.41 RDBWLB (70h/7000h):Read Black/White Low Bits

70H	RDBWLB										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
RDBWLB	R	70h	7000h	X	BKx1	BKx0	BKy1	BKy0	Wx1	Wx0	Wy1	Wy0
Description	This command reads the lowest bits of black and white color characteristics. Black: Bkx and Bky White: Wx and Wy											
Restriction	--											

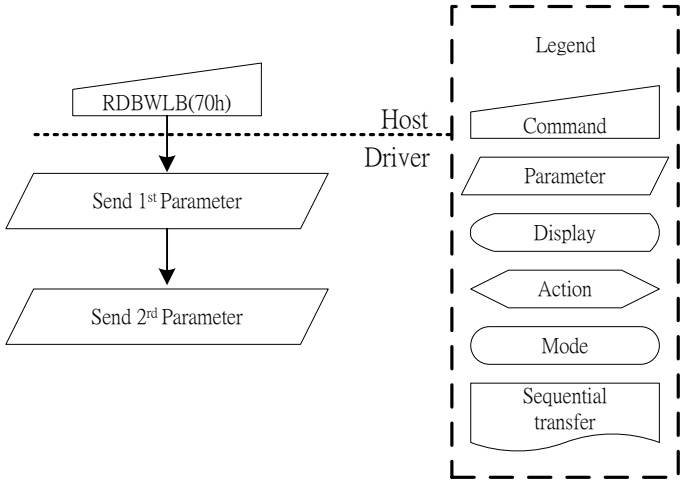
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	XXh
S/W Reset	XXh
H/W Reset	XXh

Flow Chart



12.2.42 RDBkx (71h/7100h):Read Bkx

71H	RDBkx											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
RDBkx	R	71h	7100h	X	BKx[9:2]							
Description	This command reads the Bkx bits (Bkx [9:2]) of black color characteristics.											
Restriction	Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.											

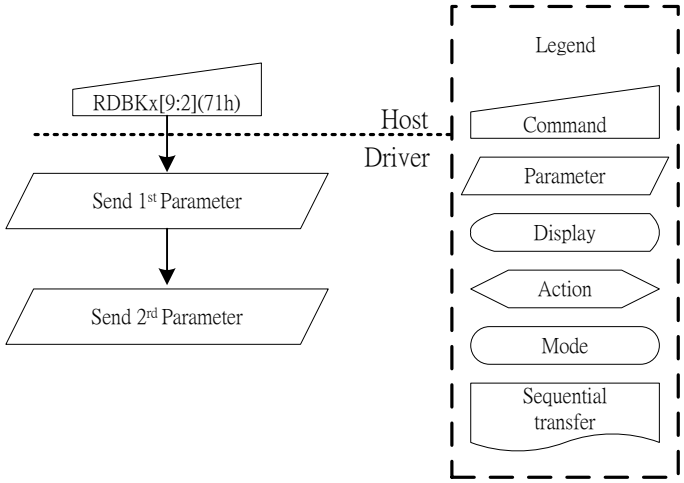
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	XXh
S/W Reset	XXh
H/W Reset	XXh

Flow Chart



12.2.43 RDBky (72h/7200h):Read Bky

<table>
<tr><td>72H</td><td colspan="12">RDBky</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>RDBky</td><td>R</td><td>72h</td><td>7200h</td><td>X</td><td colspan="8">BKy[9:2]</td></tr>
<tr><td>Description</td><td colspan="12">This command reads the Bkx bits (Bky [9:2]) of black color characteristics.</td></tr>
<tr><td>Restriction</td><td colspan="12">Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.</td></tr>
<tr><td>Register availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value (D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>XXh</td></tr>
<tr><td>S/W Reset</td><td>XXh</td></tr>
<tr><td>H/W Reset</td><td>XXh</td></tr>
</table>
</td></tr>
</table>

12.2.44 RDWx (73h/7300h):Read Wx

<table>
<tr><td>73H</td><td colspan="12">RDWx</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>RDWx</td><td>R</td><td>72h</td><td>7200h</td><td>X</td><td colspan="8">Wx[9:2]</td></tr>
<tr><td>Description</td><td colspan="12">This command reads the Wx bits (Bky [9:2]) of black color characteristics.</td></tr>
<tr><td>Restriction</td><td colspan="12">Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.</td></tr>
<tr><td>Register availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value (D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>XXh</td></tr><tr><td>S/W Reset</td><td>XXh</td></tr><tr><td>H/W Reset</td><td>XXh</td></tr></table></td></tr>
</table>

12.2.45 RDWy (74h/7400h):Read Wy

<table>
<tr><td>74H</td><td colspan="12">RDWy</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>RDWy</td><td>R</td><td>74h</td><td>7400h</td><td>X</td><td colspan="8">Wy[9:2]</td></tr>
<tr><td>Description</td><td colspan="12">This command reads the Wx bits (Bky [9:2]) of black color characteristics.
“-“ Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="12">Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.</td></tr>
<tr><td>Register availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value (D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>XXh</td></tr><tr><td>S/W Reset</td><td>XXh</td></tr><tr><td>H/W Reset</td><td>XXh</td></tr></table></td></tr>
</table>

12.2.46 RDRGLB (75h/7500h):Read Red/Green Low Bits

75H	RDRGLB											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
RDRGLB	R	75h	7500h	X	Rx1	Rx0	Ry1	Ry0	Gx1	Gx0	Gy1	Gy0
Description	This command reads the lowest bits of red and green color characteristics. Red: Rx and Ry Green: Gx and Gy											
Restriction	Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.											

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	XXh
S/W Reset	XXh
H/W Reset	XXh

12.2.47 RDRx (76h/7600h):Read Rx

<table>
<tr><td>76H</td><td colspan="12">RDRx</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>RDRx</td><td>R</td><td>76h</td><td>7600h</td><td>X</td><td colspan="8">Rx[9:2]</td></tr>
<tr><td>Description</td><td colspan="12">This command reads the Rx bits (Rx [9:2]) of red color characteristics.</td></tr>
<tr><td>Restriction</td><td colspan="12">Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.</td></tr>
<tr><td>Register availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value (D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>XXh</td></tr><tr><td>S/W Reset</td><td>XXh</td></tr><tr><td>H/W Reset</td><td>XXh</td></tr></table></td></tr>
</table>

12.2.48 RDRy (77h/7700h):Read Ry

<table>
<tr><td>77H</td><td colspan="12">RDRy</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>RDRy</td><td>R</td><td>77h</td><td>7700h</td><td>X</td><td colspan="8">Ry[9:2]</td></tr>
<tr><td>Description</td><td colspan="12">This command reads the Rx bits (Ry [9:2]) of red color characteristics.</td></tr>
<tr><td>Restriction</td><td colspan="12">Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.</td></tr>
<tr><td>Register availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value (D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>XXh</td></tr><tr><td>S/W Reset</td><td>XXh</td></tr><tr><td>H/W Reset</td><td>XXh</td></tr></table></td></tr>
</table>

12.2.49 RDGx (78h/7800h):Read Gx

<table>
<tr><td>78H</td><td colspan="12">RDGx</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>RDGx</td><td>R</td><td>77h</td><td>7700h</td><td>X</td><td colspan="8">Gx[9:2]</td></tr>
<tr><td>Description</td><td colspan="12">This command reads the Rx bits (Gx [9:2]) of red color characteristics.</td></tr>
<tr><td>Restriction</td><td colspan="12">Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.</td></tr>
<tr><td>Register availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value (D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>XXh</td></tr><tr><td>S/W Reset</td><td>XXh</td></tr><tr><td>H/W Reset</td><td>XXh</td></tr></table></td></tr>
</table>

12.2.50 RDGy (79h/7900h):Read Gy

<table>
<tr><td>79H</td><td colspan="12">RDGy</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>RDGy</td><td>R</td><td>79h</td><td>7900h</td><td>X</td><td colspan="8">Gy[9:2]</td></tr>
<tr><td>Description</td><td colspan="12">This command reads the Gx bits (Gx [9:2]) of red color characteristics.</td></tr>
<tr><td>Restriction</td><td colspan="12">Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.</td></tr>
<tr><td>Register availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value (D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>XXh</td></tr><tr><td>S/W Reset</td><td>XXh</td></tr><tr><td>H/W Reset</td><td>XXh</td></tr></table></td></tr>
</table>

12.2.51 RDBALB (7Ah/7A00h):Read Blue/A Color Low Bits

7AH	RDBALB										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
RDBALB	R	7Ah	7A00h	X	Bx1	Bx0	By1	By0	Ax1	Ax0	Ay1	Ay0
Description	This command reads the lowest bits of blue and A color color characteristics. Blue: Bx and By A color: Ax and Ay											
Restriction	Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.											
Register availability												

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	XXh
S/W Reset	XXh
H/W Reset	XXh

12.2.52 RDBx (7Bh/7B00h):Read Bx

<table>
<tr><td>7BH</td><td colspan="11">RDBx</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>RDBx</td><td>R</td><td>7Bh</td><td>7B00h</td><td>X</td><td colspan="7">Bx[9:2]</td></tr>
<tr><td>Description</td><td colspan="11">This command reads the Bx bits (Bx [9:2]) of red color characteristics.</td></tr>
<tr><td>Restriction</td><td colspan="11">Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.</td></tr>
<tr><td>Register availability</td><td colspan="11">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="11">
<table>
<tr><th>Status</th><th>Default Value (D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>XXh</td></tr>
<tr><td>S/W Reset</td><td>XXh</td></tr>
<tr><td>H/W Reset</td><td>XXh</td></tr>
</table>
</td></tr>
</table>

12.2.53 RDBy (7Ch/7C00h):Read By

<table>
<tr><td>7CH</td><td colspan="12">RDBy</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>RDBx</td><td>R</td><td>7Ch</td><td>7C00h</td><td>X</td><td colspan="8">By[9:2]</td></tr>
<tr><td>Description</td><td colspan="12">This command reads the By bits (By [9:2]) of red color characteristics.</td></tr>
<tr><td>Restriction</td><td colspan="12">Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.</td></tr>
<tr><td>Register availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value (D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>XXh</td></tr>
<tr><td>S/W Reset</td><td>XXh</td></tr>
<tr><td>H/W Reset</td><td>XXh</td></tr>
</table>
</td></tr>
</table>

12.2.54 RDAx (7Dh/7D00h):Read Ax

<table>
<tr><td>7DH</td><td colspan="12">RDAx</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>RDAx</td><td>R</td><td>7Dh</td><td>7D00h</td><td>X</td><td colspan="8">Ax[9:2]</td></tr>
<tr><td>Description</td><td colspan="12">This command reads the Ax bits (Ax [9:2]) of red color characteristics.</td></tr>
<tr><td>Restriction</td><td colspan="12">Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.</td></tr>
<tr><td>Register availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value (D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>XXh</td></tr><tr><td>S/W Reset</td><td>XXh</td></tr><tr><td>H/W Reset</td><td>XXh</td></tr></table></td></tr>
</table>

12.2.55 RDAy (7Eh/7E00h):Read Ay

<table>
<tr><td>7EH</td><td colspan="12">RDAy</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>RDAy</td><td>R</td><td>7Dh</td><td>7D00h</td><td>X</td><td colspan="8">Ay[9:2]</td></tr>
<tr><td>Description</td><td colspan="12">This command reads the Ay bits (Ay [9:2]) of red color characteristics.</td></tr>
<tr><td>Restriction</td><td colspan="12">Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.</td></tr>
<tr><td>Register availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value (D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>XXh</td></tr><tr><td>S/W Reset</td><td>XXh</td></tr><tr><td>H/W Reset</td><td>XXh</td></tr></table></td></tr>
</table>

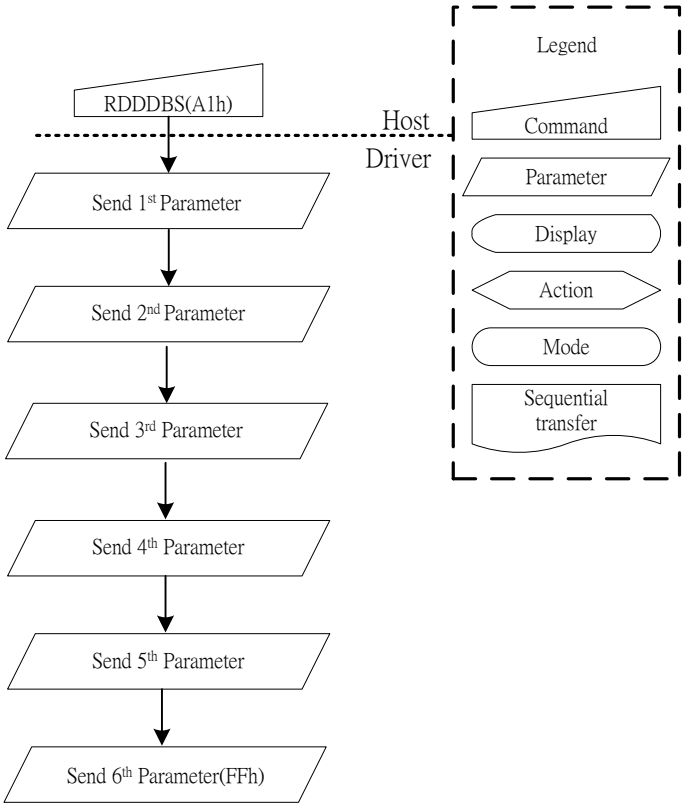
12.2.56 RDDDBS (A1h/A100h): Read DDB Start

A1H	RDDDBS											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
RDDDBS	R	A1h	A100h	X	0x88							
			A101h		0x02							
			A102h		MID[15:8]							
			A103h		MID[7:0]							
			A104h		8'hff							
Description	This command reads the supplier identification and display module mode/revision information. Parameter 1: the ID of IC.(0x88). Parameter 2: the ID of IC.(0x02). Parameter 3: MRID [7:0] LCD module/driver ID. Parameter 4: MRID [15:8] IC version code. Parameter 5: FFh - Exit code – there is no more data in the Descriptor Block This read sequence can be interrupted by any command and it can be continued by the Read DDB Continue (A8h) command. For example, RDDDBS => 1st parameter has been sent => 2nd parameter has been sent => interrupt => RDDDBC => 3rd parameter of the RDDDBS has been sent.											
Restriction												
Register availability												

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	XXh
S/W Reset	XXh
H/W Reset	XXh

Flow Chart	

12.2.57 RDDDBC (A8h/A800h): Read DDB Continue

A8H	RDDDBC											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
RDDDBC	R	A8h	A800h	X	SID[15:8]							
			A801h		SID[7:0]							
			A802h		MID[15:8]							
			A803h		MID[7:0]							
			A804h		8'hff							
Description	This command is used to read the supplier's identification and revision information from the point where RDDDBS (A1h) was interrupted by another command.											
Restriction												

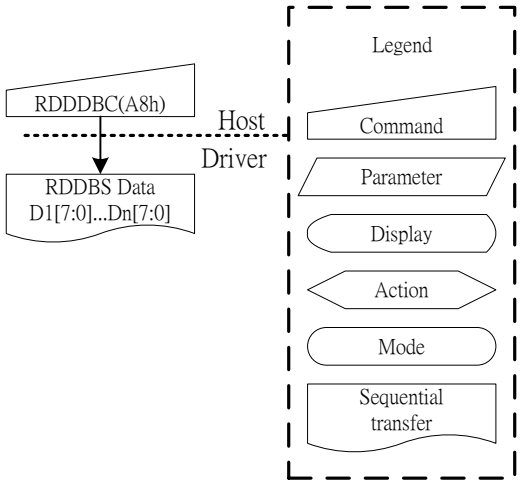
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	XXh
S/W Reset	XXh
H/W Reset	XXh

Flow Chart



12.2.58 RDFCS (AAh/AA00h): Read First Checksum

AAH	RDFCS										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
RDFCS	R	7Dh	7D00h	X	FCS[7:0]							
Description	This command reads the first checksum calculated from registers of the User's area and the Frame Memory after the write access to those registers and/or Frame Memory has been done.											
Restriction	Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.											

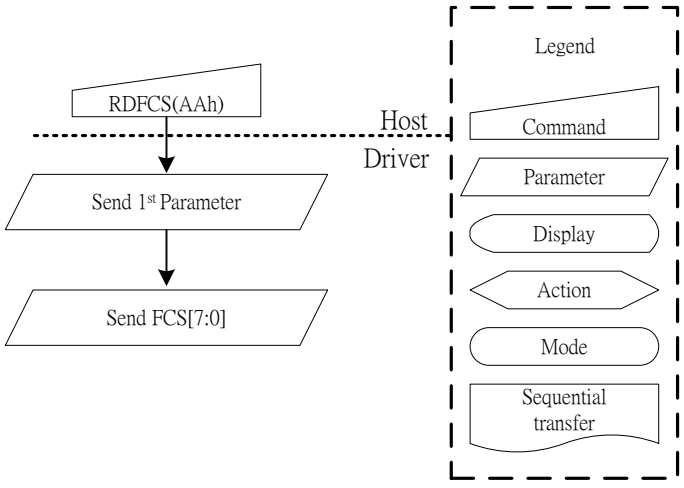
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	78h
S/W Reset	78h
H/W Reset	78h

Flow Chart



12.2.59 RDCCS (AFh/AF00h): Read Continue Checksum

AFH	RDCCS											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
RDCCS	R	AFh	AF00h	X	CCS[7:0]							
Description	This command reads the following checksum that is calculated continuously after the first checksum from registers of the User's area and the Frame Memory after the write access to those registers and/or Frame Memory is done.											
Restriction	It is necessary to wait 300ms after the last write access to registers of the User's area before this checksum value can be read the first time. Only the 2nd parameter is sent on the DSI; the 1st parameter is not sent.											

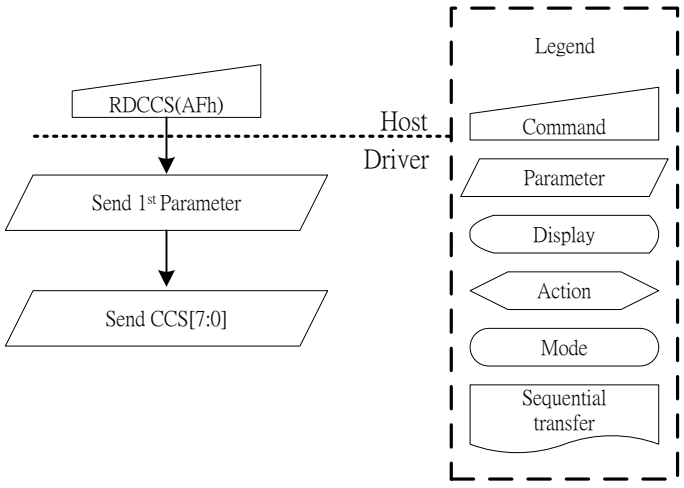
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	78h
S/W Reset	78h
H/W Reset	78h

Flow Chart



12.2.60 RDID1 (DAh/DA00h): Read ID1

DAH	RDID1										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
RDID1	R	DAh	DA00h	X	ID1[7:0]							
Description	-This read byte identifies the LCD module's manufacturer.											
Restriction												

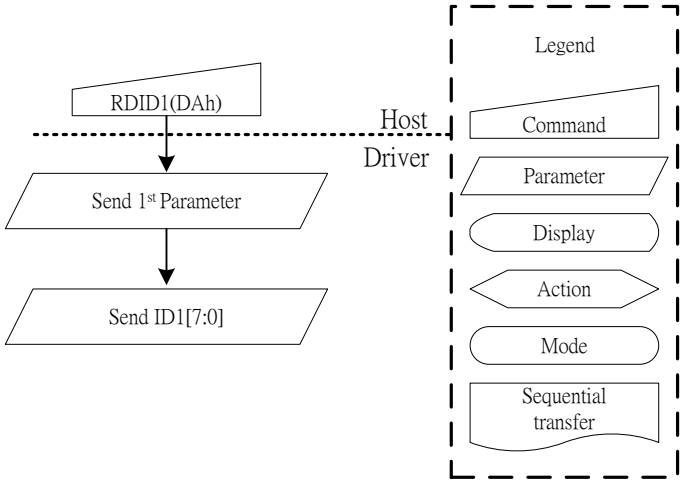
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	xxh
S/W Reset	xxh
H/W Reset	xxh

Flow Chart



12.2.61 RDID2 (DBh/DB00h): Read ID2

DBH	RDID2										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
RDID2	R	DBh	DB00h	X	ID2[7:0]							
Description	-This read byte identifies the LCD module's manufacturer.											
Restriction												

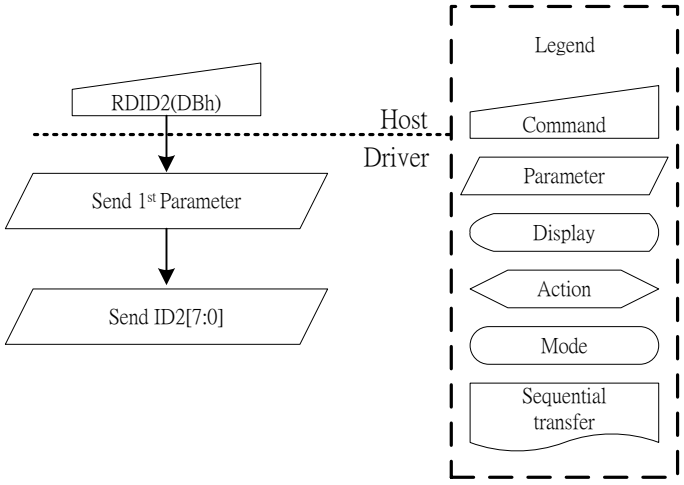
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	xxh
S/W Reset	xxh
H/W Reset	xxh

Flow Chart



12.2.62 RDID3 (DCh/DC00h): Read ID3

DCH	RDID3										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
RDID3	R	DCh	DC00h	X	ID3[7:0]							
Description	-This read byte identifies the LCD module's manufacturer.											
Restriction												

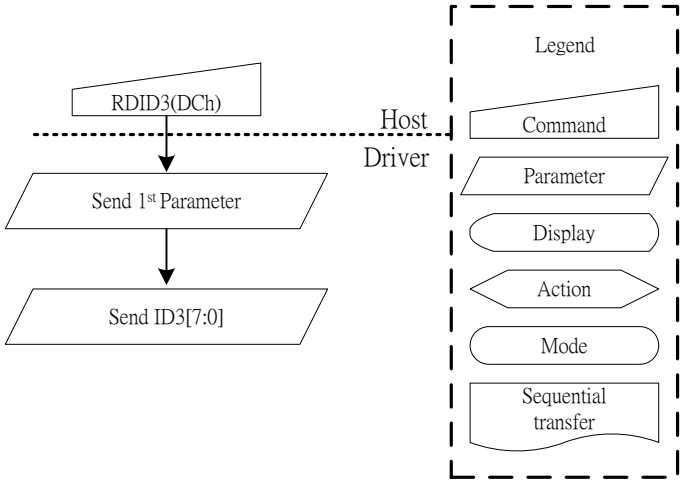
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	xxh
S/W Reset	xxh
H/W Reset	xxh

Flow Chart



12.3 System Function Command Table 2

Instruction	Address		R/W	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Function
	MIPI	SPI-16											
CN2BKxSEL	FFh	FF00h	W	5	0	1	1	1	0	1	1	1	Command2_BKx Function Selection
		FF01h			0	0	0	0	0	0	0	1	
		FF02h			--	--	--	--	--	--	--	--	
		FF03h			--	--	--	--	--	--	--	--	
		FF04h			0	0	0	CN2	0	0	0	BKSEL	

Command2_BK0

Instruction	Address		R/W/C	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Function
	MIPI	SPI-16											
PVGAMCTRL	B0h	B000h	W	16	AJ0P[1:0]		--	--	VC0P[3:0]				Positive Voltage Gamma Control
		B001h			AJ1P[1:0]		VC4P[5:0]						
		B002h			AJ2P[1:0]		VC8P[5:0]						
		B003h			--	--	--	VC16P[4:0]					
		B004h			AJ3P[1:0]		--	VC24P[4:0]					
		B005h			--	--	--	--	VC52P[3:0]				
		B006h			--	--	VC80P[5:0]						
		B007h			--	--	--	--	VC108P[3:0]				
		B008h			--	--	--	--	VC147P[3:0]				
		B009h			--	--	VC175P[5:0]						
		B00Ah			--	--	--	--	VC203P[3:0]				
		B00Bh			AJ4P[1:0]		--	VC231P[4:0]					
		B00Ch			--	--	--	VC239P[4:0]					
		B00Dh			AJ5P[1:0]		VC247P[5:0]						
		B00Eh			AJ6P[1:0]		VC251P[5:0]						
		B00Fh			AJ7P[1:0]		--	VC255P[4:0]					
NVGAMCTRL	B1h	B100h	W	16	AJ0N[1:0]		--	--	VC0N[3:0]				Negative Voltage Gamma Control
		B101h			AJ1N[1:0]		VC4N[5:0]						
		B102h			AJ2N[1:0]		AJ2P[1:0]						
		B103h			--	--	--	VC16N[4:0]					
		B104h			--	--	--	VC24N[4:0]					
		B105h			--	--	--	--	VC52N[3:0]				
		B106h			--	--	VC80N[5:0]						
		B107h			--	--	--	--	VC108N[3:0]				
		B108h			--	--	--	--	VC147N[3:0]				

Instruction	Address		R/W/C	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Function
	MIPI	SPI-16											
		B109h			--	--	VC175N[5:0]						
		B10Ah			--	--	--	--	VC203N[3:0]				
		B10Bh			AJ4N[1:0]		--	VC231N[4:0]					
		B10Ch			--	--	--	VC239N[4:0]					
		B10Dh			AJ5N[1:0]		AJ5P[1:0]						
		B10Eh			AJ6N[1:0]		AJ6P[1:0]						
		B10Fh			AJ7N[1:0]		--	VC255N[4:0]					
DGMEN	B8	B800h	W	1	0	0	0	DGM_ON	0	0	0	0	Digital Gamma Enable
DGMLUTR	B9	B900	W	130	P0[7:0]								Digital Gamma Look-up Table for Red
		B901			--	--	--	--	--	--	P0[9:8]		
		B902			--	--	--	--	--	--	P4[1:0]		
		B903			--	--	--	--	--	--	--	--	
		B904			P8[7:0]								
		B905			--	--	--	--	--	--	P8[9:8]		
		B906			--	--	--	--	--	--	P12[1:0]		
		B907			--	--	--	--	--	--	--	--	
		:			:								
		:			:								
		B97C			P248[7:0]								
		B97D			--	--	--	--	--	--	P248[9:8]		
		B97E			--	--	--	--	--	--	P252[1:0]		
		B97F			--	--	--	--	--	--	--	--	
		B980			P255[7:0]								
		B981			--	--	--	--	--	--	P255[9:8]		
DGMLUTB	BA	BA00	W	130	P0[7:0]								Digital Gamma Look-up Table for Blue
		BA01			--	--	--	--	--	--	P0[9:8]		
		BA02			--	--	--	--	--	--	P4[1:0]		
		BA03			--	--	--	--	--	--	--	--	
		BA04			P8[7:0]								
		BA05			--	--	--	--	--	--	P8[9:8]		
		BA06			--	--	--	--	--	--	P12[1:0]		
		BA07			--	--	--	--	--	--	--	--	
		:			:								
		:			:								

Instruction	Address		R/W/C	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Function
	MIPI	SPI-16											
		BA7C			P248[7:0]								
		BA7D			--	--	--	--	--	--	P248[9:8]		
		BA7E			--	--	--	--	--	--	P252[1:0]		
		BA7F			--	--	--	--	--	--	--	--	
		BA80			P255[7:0]								
		BA81			--	--	--	--	--	--	P255[9:8]		
PWM_CLK	BC	BC00	W	1	0	0	0	1	1	Pwm_clk_sel[2:0]			PWM CLK select
LNESET	C0	C000	W	2	LDE_EN	Line[6:0]							Display Line setting
		C001		2	--	--	--	--	--	--	Line_Delta[1:0]		
PORCTRL	C1	C100	W	2	VBP[7:0]								Porch control
		C101		2	VFP[7:0]								
INVSEL	C2	C200	W	2	0	0	1	1	0	NLINV[2:0]			Inversion selection & Frame Rate Control
		C201		2	--	--	--	RTNI[4:0]					
RGBCTRL	C3	C300	W	3	DE/HV	--	--	--	VSP	HSP	DP	EP	RGB control
		C301		3	HBP_HVRGB[7:0]								
		C302		3	VBP_HVRGB[7:0]								
PARCTRL	C5	C500	W	4	PTSA[7:0]								Partial mode Control
		C501		4	--	--	--	--	--	--	PTSA[9:8]		
		C502		4	PTEA[7:0]								
		C503		4	--	--	--	--	--	--	PTEA[9:8]		
SDIR	C7	C700	W	1	--	--	--	--	--	SS	--	--	Source direction control
PDOTSET	C8	C800	W	1	Z_EN	Z_SDM1S	Z_GltoR	--	--	--	--	--	Pesudo-Dot inversion driving setting
COLCTRL	CD	CD00	W	1	--	--	INV_LED PWM	INV_LED ON	MDT	EPF[2:0]			Color Control
SSCTRL	CE	CE00	W	1	DSSE	0	DSSRG[1:0]		0	1	0	0	Spread spectrum Control
SECTRL	E0	E000	W	1	--	--	--	SRE	SRE_alpha[3:0]				Sunlight Readable Enhancement
NRCTRL	E1	E100	W	1	--	--	--	NRE	--	--	NR_md[1:0]		Noise Reduce Control
SECTRL	E2	E200	W	1	--	--	--	SE	Y_gain[3;0]				Sharpness Control
CCCTRL	E3	E300	W	1	--	--	--	--	--	--	--	CCE	Color Calibration Control
SKCTRL	E4	E400	W	1	--	--	--	SKE	--	--	Skin_ce_mid[1:0]		Skin Tone Preservation Control
NVMSETE	EA	EA00	W	1	--	--	--	--	--	--	--	ADEN	NVM address Setting Enable
CABCCTRL	EE	EE00	W	1	'--	'--	'--	LEDPWR SEL	'--	'--	'--	LED_EN	CABC Control

Command2_BK1

Instruction	Address		R/W/C	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Function
	MIPI	SPI-16											
VRHS	B0	B000	W	1	VRHA[7:0]								Vop amplitude setting
VCOMS	B1	B100	W	1	VCOM[7:0]								VCOM amplitude setting
VGHSS	B2	B200	W	1	--	--	--	--	VGHSS[3:0]				VGH Voltage setting
TESCMD	B3	B300	W	1	1	--	--	--	--	0	0	0	TEST Command Setting
VGLS	B5	B500	W	1	0	1	--	--	VGLS[3:0]				VGL Voltage setting
VRHDV	B6	B600	W	1	0	VRH_DV[6:0]							VRH_DV Voltage setting
PWCTRL1	B7	B700	W	1	AP[1:0]		--	--	APIS[1:0]		APOS[1:0]		Power Control 1
PWCTRL2	B8	B800	W	1	--	--	AVDD[1:0]		--	--	AVCL[1:0]		Power Control 2
PWCTRL3	B9	B900	W	1	--	--	SVPO_PUM		--	--	SVNO_PUM		Power Control 3
PCLKS 1	BA	BA00	W	1	--	--	STP4CKS[1:0]		--	--	STP1CKS[1:0]		Power pumping clk selection 1
PCLKS 2	BB	BB00	W	1	--	--	--	--	--	--	SBSTCKS[1:0]		Power pumping clk selection 2
PCLKS 3	BC	BC00	W	1	--	--	STP3CKS[1:0]		STP2PCKS[1:0]		STP2SCKS[1:0]		Power pumping clk selection 3
PDR1	C1	C100	W	1	0	1	1	1	T2D				Source pre_drive timing set1
PDR2	C2	C200	W	1	0	1	1	1	T3D				Source pre_drive timing set2
MIPISET 1	D0	D000	W	1	1	0	0	0	EOTP_EN	0	ERR_SEL[1:0]		MIPI Setting 1
MIPISET 2	D1	D100	W	4	Mpc_tlpx1[3:0]				Mpc_tlpx0[3:0]				MIPI Setting 2
		D101			Mpc_txtimeadj[3:0]				Mpc_tlpx2[3:0]				
		D102			--	--	--	--	Mpc_ttago[3:0]				
		D103			--	--	--	--	Mpc_ttaget[3:0]				
MIPISET 3	D2	D200	W	1	--	--	1	1	PHY_ttasure[3:0]				MIPI Setting 3
MIPISET 4	D3	D300	W	2	--	--	--	--	--	PHY_CSK[2:0]			MIPI Setting 4
		D301			--	PHY_dsk1[2:0]			--	PHY_dsk0[2:0]			

Command2_BK3

Instruction	Address		R/W/C	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Function
	MIPI	SPI-16											
NVMEN	C8	C800	W	4	0	1	1	1	0	1	1	1	NVM Enable
		C801			0	0	0	0	0	0	0	1	
		C802			1	1	1	0	1	1	1	0	
		C803			0	0	0	0	0	1	0	0	
NVMSET	CA	CA00	W	3	--						PA [9:8]		NVM manual control Setting
		CA01			PA [7:0]								
		CA02			PDIN [7:0]								

Instruction	Address		R/W/C	PNUM	D7	D6	D5	D4	D3	D2	D1	D0	Function
	MIPI	SPI-16											
PROMACT	CC	CC01	W	1	1	0	1	0	1	0	1	0	NVM Program Active

12.3.1 CND2BKxSEL (FFh/FF00h): Command2 BKx Selection

FFH	CND2BKxSEL										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
CN2BKxSEL	W	FFh	FF00h	X	0	1	1	1	0	1	1	1
	W		FF01h	X	0	0	0	0	0	0	0	1
	W		FF02h	X	0	0	0	0	0	0	0	0
	W		FF03h	X	0	0	0	0	0	0	0	0
	W		FF04h	X	0	0	0	CN2	0	0	0	BKxSEL

Description

This command is used to select the function of Command BK0 or Command BK1.

When CN2=’1’ enable the BK function of Command2, CN2=’0’ disable the BK function of Command2.

BKxSEL	BKx Function Select
00h	BK0
01h	BK1
03h	BK3

Restriction

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

12.3.2 Command 2 BK0 Function

12.3.2.1 PVGAMCTRL (B0h/B000h): Positive Voltage Gamma Control

B0H	PVGAMCTRL (BK0)										
Inst / Para	R/W	Address MIPI	Address SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
PVGAMCTRL	W	B0h	B000h	X	AJ0P[1:0]		--	--	VC0P[3:0]			
	W		B001h	X	AJ1P[1:0]		VC4P[5:0]					
	W		B002h	X	AJ2P[1:0]		VC8P[5:0]					
	W		B003h	X	--	--	--	VC16P[4:0]				
	W		B004h	X	AJ3P[1:0]		--	VC24P[4:0]				
	W		B005h	X	--	--	--	--	VC52P[3:0]			
	W		B006h	X	--	--	VC80P[5:0]					
	W		B007h	X	--	--	--	--	VC108P[3:0]			
	W		B008h	X	--	--	--	--	VC147P[3:0]			
	W		B009h	X	--	--	VC175P[5:0]					
	W		B00Ah	X	--	--	--	--	VC203P[3:0]			
	W		B00Bh	X	AJ4P[1:0]		--	VC231P[4:0]				
	W		B00Ch	X	--	--	--	VC239P[4:0]				
	W		B00Dh	X	AJ5P[1:0]		VC247P[5:0]					
	W		B00Eh	X	AJ6P[1:0]		VC251P[5:0]					
	W		B00Fh	X	AJ7P[1:0]		'--	VC255P[4:0]				

Description

Please refer to 11.

Default value:

	Value(hex)		Value(hex)
VC0P[3:0]	00H	VC239P[4:0]	00H
VC4P[5:0]	00H	VC247P[5:0]	00H
VC8P[5:0]	00H	VC251P[5:0]	00H
VC16P[4:0]	00H	VC255P[4:0]	00H
VC24P[4:0]	00H	AJ0P[1:0]	00H
VC52P[3:0]	00H	AJ1P[1:0]	00H
VC80P[5:0]	00H	AJ2P[1:0]	00H
VC108P[3:0]	00H	AJ3P[1:0]	00H
VC147P[3:0]	00H	AJ4P[1:0]	00H
VC175P[5:0]	00H	AJ5P[1:0]	00H
VC203P[3:0]	00H	AJ6P[1:0]	00H
VC231P[4:0]	00H	AJ7P[1:0]	00H

Restriction	--

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	All “0”
S/W Reset	All “0”
H/W Reset	All “0”

12.3.2.2 NVGAMCTRL (B1h/B100h): Negative Voltage Gamma Control

B1H	NVGAMCTRL (BK0)										
Inst / Para	R/W	Address MIPI	Address SPI-16	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
NVGAMCTRL	W	B0h	B100h	X	AJ0N[1:0]		--	--	VC0N[3:0]			
	W		B101h	X	AJ1N[1:0]		VC8N[5:0]					
	W		B102h	X	AJ2N[1:0]		VC8N[5:0]					
	W		B103h	X	--	--	--	VC16N[4:0]				
	W		B104h	X	AJ3N[1:0]		--	VC24N[4:0]				
	W		B105h	X	--	--	--	--	VC52N[3:0]			
	W		B106h	X	--	--	VC80N[5:0]					
	W		B107h	X	--	--	--	--	VC108N[3:0]			
	W		B108h	X	--	--	--	--	VC147N[3:0]			
	W		B109h	X	--	--	VC175N[5:0]					
	W		B10Ah	X	--	--	--	--	VC203N[3:0]			
	W		B10Bh	X	AJ4N[1:0]		--	VC231N[4:0]				
	W		B10Ch	X	--	--	--	VC239N[4:0]				
	W		B10Dh	X	AJ5N[1:0]		VC247N[5:0]					
	W		B10Eh	X	AJ6N[1:0]		VC251N[5:0]					
	W		B10Fh	X	AJ7N[1:0]		'--	VC255N[4:0]				

Description

Please refer to 11.

Default value:

	Value(hex)		Value(hex)
VC0N[3:0]	00H	VC239N[4:0]	00H
VC4N[5:0]	00H	VC247N[5:0]	00H
VC8N[5:0]	00H	VC251N[5:0]	00H
VC16N[4:0]	00H	VC255N[4:0]	00H
VC24N[4:0]	00H	AJ0N[1:0]	00H
VC52N[3:0]	00H	AJ1N[1:0]	00H
VC80N[5:0]	00H	AJ2N[1:0]	00H
VC108N[3:0]	00H	AJ3N[1:0]	00H
VC147N[3:0]	00H	AJ4N[1:0]	00H
VC175N[5:0]	00H	AJ5N[1:0]	00H
VC203N[3:0]	00H	AJ6N[1:0]	00H
VC231N[4:0]	00H	AJ7N[1:0]	00H

Restriction	--

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	All “0”
S/W Reset	All “0”
H/W Reset	All “0”

12.3.2.3 DGMEN (B8h/B800h): Digital Gamma Enable

B8H	DGMEN (BK0)										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
DGMEN	W	B8h	B800h	X	0	0	0	DGM_ON	0	0	0	0
Description	**DGM_ON**:Digital Gamma Enable DGM_ON=”0” , disable this function. DGM_ON=”1” , enable this function.											
Restriction	--											

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

12.3.2.4 DGMLUTR (B9h/B900h): Digital Gamma Look-up Table for Red

B9H	DGMLUTR (BK0)											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
DGMLUTB	W	B9h	B900h	X	P0[7:0]							
	W		B901h	X	--	--	--	--	--	--	P0[9:8]	
	W		B902h	X	--	--	--	--	--	--	P4[1:0]	
	W		B903h	X	--	--	--	--	--	--	--	--
	W		B904h	X	P8[7:0]							
	W		B905h	X	--	--	--	--	--	--	P8[9:8]	
	W		B906h	X	--	--	--	--	--	--	P12[1:0]	
	W		B907h	X	--	--	--	--	--	--	--	--
	W		:	X	:							
	W		:	X	:							
	W		B97Ch	X	P248[7:0]							
	W		B97Dh	X	--	--	--	--	--	--	P248[9:8]	
	W		B97Eh	X	--	--	--	--	--	--	P252[1:0]	
	W		B97Fh	X	--	--	--	--	--	--	--	--
	W		B980h	X	P255[7:0]							
	W		B981h	X	--	--	--	--	--	--	P255[9:8]	
Description	Digital Gamma Look-up Table for Red											
Restriction	--											

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	All “0”
S/W Reset	All “0”
H/W Reset	All “0”

12.3.2.5 DGMLUTB (BAh/BA00h): Digital Gamma Look-up Table for Blue

BAH	DGMLUTB (BK0)											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
DGMLUTB	W	BAh	BA00h	X	P0[7:0]							
	W		BA01h	X	--	--	--	--	--	--	P0[9:8]	
	W		BA02h	X	--	--	--	--	--	--	P4[1:0]	
	W		BA03h	X	--	--	--	--	--	--	--	--
	W		BA04h	X	P8[7:0]							
	W		BA05h	X	--	--	--	--	--	--	P8[9:8]	
	W		BA06h	X	--	--	--	--	--	--	P12[1:0]	
	W		BA07h	X	--	--	--	--	--	--	--	--
	W		:	X	:							
	W		:	X	:							
	W		BA7Ch	X	P248[7:0]							
	W		BA7Dh	X	--	--	--	--	--	--	P248[9:8]	
	W		BA7Eh	X	--	--	--	--	--	--	P252[1:0]	
	W		BA7Fh	X	--	--	--	--	--	--	--	--
	W		BA80h	X	P255[7:0]							
	W		BA81h	X	--	--	--	--	--	--	P255[9:8]	
Description	Digital Gamma Look-up Table for Blue											
Restriction	--											

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	All “0”
S/W Reset	All “0”
H/W Reset	All “0”

12.3.2.6 PWM CLK SEL(BCh/BC00h):PWM CLK select

<table>
<tr><td>BCH</td><td colspan="12">PWM CLK SEL (BK0)</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td></td><td>W</td><td></td><td>BC00h</td><td>X</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td colspan="3">PWM CLK SEL[2:0]</td></tr>
<tr><td>Description</td><td colspan="12">PWM CLK SEL[2:0] : PWM CLK select.
<table>
<tr><td></td><td>Value(hex)</td><td></td></tr>
<tr><td>PWM CLK SEL[2:0]</td><td>00H</td><td>Clk/1</td></tr>
<tr><td>PWM CLK SEL[2:0]</td><td>01H</td><td>Clk/2</td></tr>
<tr><td>PWM CLK SEL[2:0]</td><td>02H</td><td>Clk/4</td></tr>
<tr><td>PWM CLK SEL[2:0]</td><td>03H</td><td>Clk/8</td></tr>
<tr><td>PWM CLK SEL[2:0]</td><td>04H</td><td>Clk/16</td></tr>
<tr><td>PWM CLK SEL[2:0]</td><td>05H</td><td>Clk/32</td></tr>
<tr><td>PWM CLK SEL[2:0]</td><td>06H</td><td>Clk/64</td></tr>
<tr><td>PWM CLK SEL[2:0]</td><td>07H</td><td>Clk/128</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">--</td></tr>
<tr><td>Register availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value (D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>1fh</td></tr>
<tr><td>S/W Reset</td><td>1fh</td></tr>
<tr><td>H/W Reset</td><td>1fh</td></tr>
</table></td></tr>
</table>

12.3.2.7 LNESET (C0h/C000h): Display Line Setting

<table>
<tr><td>C0H</td><td colspan="11">LNESET (BK0)</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td rowspan="2">LNESET</td><td>W</td><td rowspan="2">C0h</td><td>C000h</td><td>X</td><td>LDE_EN</td><td colspan="6">Line[6:0]</td></tr>
<tr><td>W</td><td>C001h</td><td>X</td><td>--</td><td>--</td><td>--</td><td>--</td><td>--</td><td>--</td><td colspan="2">Line_delta[1:0]</td></tr>
<tr><td>Description</td><td colspan="11">Line[6:0] : display line setting
LDE_EN : add extra-line enable
LDE_EN=”0”,no add delta line , NL= (Line[6:0]+1)*8
EX:(C0:0x6b,0x00)➔ ((0x6b+1) x 8)=864;
LDE_EN=”1”,add delta line , NL=(Line[6:0]+1)*8+ Line_delta[1:0]*2
EX: (C0:0xe9,0x03)➔((0x69+1) x8) + (3x2)=854
SCNL= NL+VBP+VFP</td></tr>
<tr><td>Restriction</td><td colspan="11">--</td></tr>
<tr><td>Register availability</td><td colspan="11"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="11"><table><tr><th>Status</th><th>Default Value (D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>6bh/00h</td></tr><tr><td>S/W Reset</td><td>6bh/00h</td></tr><tr><td>H/W Reset</td><td>6bh/00h</td></tr></table></td></tr>
</table>

12.3.2.8 PORCTRL (C1h/C100h):Porch Control

C1H	PORCTRL (BK0)											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
PORCTRL	W	C1h	C100h	X	VBP[7:0]							
	W		C101h	X	VFP[7:0]							
Description	**VBP[7:0]:** Back-Porch Vertical line setting for display. **VFP[7:0]:** Front-Porch Vertical line setting for display.											
Restriction	--											

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	04h/02h
S/W Reset	04h/02h
H/W Reset	04h/02h

12.3.2.9 INVSET (C2h/C200h):Inversion selection & Frame Rate Control

<table>
<tr><td>C2H</td><td colspan="12">INVSET (BK0)</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td rowspan="2">INVSET</td><td>W</td><td rowspan="2">C2h</td><td>C200h</td><td>X</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td colspan="3">NLINV[2:0]</td></tr>
<tr><td>W</td><td>C201h</td><td>X</td><td>--</td><td>--</td><td>--</td><td colspan="5">RTNI[4:0]</td></tr>
<tr><td>Description</td><td colspan="12">NLINV[2:0]:Inversion Selection
<table><tr><td>NLINV[2:0]</td><td>Inversion</td></tr><tr><td>0</td><td>1 Dot</td></tr><tr><td>1</td><td>2 Dot</td></tr><tr><td>7</td><td>Column</td></tr></table>RTNI[4:0]:minimum number of pclk in each line
PCLK=512+(RTNI[4:0]x16)</td></tr>
<tr><td>Restriction</td><td colspan="12">--</td></tr>
<tr><td>Register availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value (D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>10h/00h</td></tr><tr><td>S/W Reset</td><td>10h/00h</td></tr><tr><td>H/W Reset</td><td>10h/00h</td></tr></table></td></tr>
</table>

12.3.2.10 RGBCTRL (C3h/C300h):RGB control

C3H	RGBCTRL (BK0)											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
RGBCTRL	W	C3h	C300h	X	DE/HV	--	--	--	VSP	HSP	DP	EP
	W		C301h	X	HBP_HVRGB[7:0]							
	W		C302h	X	VBP_HVRGB[7:0]							
Description	**DE/HV**:RGB Mode selection DE/HV="0",RGB DE mode. DE/HV="1",RGB HV mode. **VSP :** Sets the signal polarity of the VSYNC pin. VSP="0", Low active VSP="1", High active **HSP :** Sets the signal polarity of the HSYNC pin. HSP="0", Low active HSP="1", High active **DP :** Sets the signal polarity of the DOTCLK pin. DP = "0" The data is input on the positive edge of DOTCLK DP = "1" The data is input on the negative edge of DOTCLK **EP :** Sets the signal polarity of the ENABLE pin. EP = "0" The data DB23-0 is written when ENABLE = "1". Disable data write operation when ENABLE = "0". EP = "1" The data DB23-0 is written when ENABLE = "0". Disable data write operation when ENABLE = "1". **HBP_HVRGB[7:0]:** RGB interface Vsync back porch setting for HV mode. Minimum setting is 0x02. **HBP_HVRGB[7:0]:** RGB interface Hsync back porch setting for HV mode.											
Restriction	--											
Register availability												
Default												

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value (D7 to D0)
Power On Sequence	00h/10h/08h
S/W Reset	00h/10h/08h
H/W Reset	00h/10h/08h

12.3.2.11 PARCTRL (C5h/C500h):Partial Mode Control

C5H	PARCTRL (BK0)											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
PARCTRL	W	C5h	C500h	X	PTSA[7:0]							
	W		C501h	X	--	--	--	--	--	--	PTSA[9:8]	
	W		C502h	X	PTEA[7:0]							
	W		C503	X	-	--	--	--	--	--	PTEA[9:8]	
Description	**PTSA[9:0]**: Partial display start line address **PTEA[9:0]**: Partial display end line address											
Restriction	--											

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h/00h/5fh/03h
S/W Reset	00h/00h/5fh/03h
H/W Reset	00h/00h/5fh/03h

12.3.2.12 SDIR (C7h/C700): X-direction Control

C7H	PDOSET (BK0)											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
PDOSET	W	C7h	C500h	X	--	--	--	--	--	SS	--	--
Description	**SS**:To selection x-direction. SS=”0”,source form 0 to 479 SS=”1”,source form 479 to 0											
Restriction	--											

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

12.3.2.13 PDOSET (C8h/C800h):Pseudo-Dot inversion diving setting

C8H	PDOSET (BK0)											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
PDOSET	W	C5h	C500h	X	Z_EN	Z_SDM1	Z_Gltor	--	--	--	--	--

Description

Z_EN:To enable pseudo-dot inversion driving.

Z_EN="0",enable PDOSET setting

Z_EN="1",disable PDOSET setting

Z_SDM1: SDUM_1 or SDUM_2 enable control (for Z-inv only)

Z_SDM1="0",SDUM_2 is enable

Z_SMDL="1",SDUM_1 is enable

Z_Gltor: upper-left pixel,source drive to R-Side

Z_Gltor="0",L-side first

Z_Gltor="1",R-side first

Restriction: --

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

12.3.2.14 COLCTRL (CDh/CD00h):Color Control

CDH	COLCTRL (BK0)											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
COLCTRL	W	CDh	CD00h	X	--	--	INV_LED PWM	INV_LED _ON	MDT	EPF[2:0]		

Description

INV_LED PWM: LEDPWM polarity control.

INV_LED PWM=”0”, polarity normal.

INV_LED PWM=”1”, polarity reverse.

INV_LED_ON: LED_ON polarity control.

INV_LED_ON=”0”, polarity normal.

INV_LED_ON=”1”, polarity reverse.

MDT: RGB pixel format argument.(for 262K).See Table 17.

MDT=”0”, pixel format argument normal.

MDT=”1”, pixel collect to DB[17:0].

EPF[2:0]: end of pixel format (for 65k & 262k mode)

0:copy self MSB

1:copy G MSB

2:copy self LSB

4:FIX 0

5:FIX 1

Restriction: --

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

12.3.2.15 SSCTRL (CEh/CE00h):Spread spectrum Control

<table>
<tr><td>CEH</td><td colspan="12">SSSCTRL (BK0)</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>SSCTRL</td><td>W</td><td>CEh</td><td>CE00h</td><td>X</td><td>DSSE</td><td>0</td><td colspan="2">DSSRG[1:0]</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Description</td><td colspan="12">DSSE : Digital spread spectrum Enable.
DSSE=”0”, Digital spread spectrum disable.
DSEE=”1”, Digital spread spectrum Enable.
DSSRG[1:0]: DSS OSC maximum frequency variation range setting..
<table><tr><td>DSSRG[1:0]</td><td>Range</td></tr><tr><td>0</td><td>Disable</td></tr><tr><td>1</td><td>2.5%</td></tr><tr><td>2</td><td>5%</td></tr><tr><td>3</td><td>7.5%</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="12">--</td></tr>
<tr><td>Register availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value (D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table></td></tr>
</table>

12.3.2.16 SECTRL (E0h/E000h):Sunlight Readable Enhancement

<table>
<tr><td>E0H</td><td colspan="11">SECTRL (BK0)</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>SECTRL</td><td>W</td><td>E0h</td><td>E000h</td><td>X</td><td>--</td><td>--</td><td>--</td><td>SRE</td><td colspan="4">SRE_alpha[3:0]</td></tr>
<tr><td>Description</td><td colspan="12">SRE: Sunlight Readable Enhancement (SRE) enable control.
SRE=”0”, Sunlight Readable Enhancement disable.
SRE=”1”, Sunlight Readable Enhancement enable.
SRE_alpha:Sunlight Readable Enhancemnet (SRE) level selection
[00:0F]➔ [lower : highest]</td></tr>
<tr><td>Restriction</td><td colspan="12">--</td></tr>
<tr><td>Register availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value (D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table></td></tr>
</table>

12.3.2.17 NRCTRL (E1h/E100h):Noise Reduce Control

<table>
<tr><td>E1H</td><td colspan="12">NRCTRL (BK0)</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>NRCTRL</td><td>W</td><td>E1h</td><td>E100h</td><td>X</td><td>--</td><td>--</td><td>--</td><td>NRE</td><td></td><td></td><td colspan="2">NR_md[1:0]</td></tr>
<tr><td>Description</td><td colspan="12">NRE: Noise Reduce Function Enable Control.
NRE=”0”, Noise Reduce Function disable.
NRE=”1”, Noise Reduce Function enable.
NR_md:Noise Reduce level selection.</td></tr>
<tr><td>Restriction</td><td colspan="12">--</td></tr>
<tr><td>Register availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value (D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table></td></tr>
</table>

12.3.2.18 SECTRL (E2h/E200h):Sharpness Control

<table>
<tr><td>E2H</td><td colspan="11">SECTRL (BK0)</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>SECTRL</td><td>W</td><td>E2h</td><td>E200h</td><td>X</td><td>--</td><td>--</td><td>--</td><td>SE</td><td colspan="4">Y_gain[3:0]</td></tr>
<tr><td>Description</td><td colspan="12">SE: Sharpness Function Enable Control.
SE=”0”, Sharpness Function disable.
SE=”1”, Sharpness Function enable.
Y_gain :Sharpness level Selection.</td></tr>
<tr><td>Restriction</td><td colspan="12">--</td></tr>
<tr><td>Register availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value (D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table></td></tr>
</table>

12.3.2.19 CCCTRL (E3h/E300h):Color Calibration Control

<table>
<tr><td>E3H</td><td colspan="12">CCCTRL (BK0)</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>CCCTRL</td><td>W</td><td>E3h</td><td>E300h</td><td>X</td><td>--</td><td>--</td><td>--</td><td>--</td><td>--</td><td>--</td><td>--</td><td>CCE</td></tr>
<tr><td>Description</td><td colspan="12">CCE: Color Calibration Function Enable Control.
CCE=”0”, Color Calibration Function disable.
CCE=”1”, Color Calibration Function enable.</td></tr>
<tr><td>Restriction</td><td colspan="12">--</td></tr>
<tr><td>Register availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value (D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table></td></tr>
</table>

12.3.2.20 SKCTRL (E4h/E400h):Skin Tone Preservation Control

E4H	SKCTRL (BK0)										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
SKCTRL	W	E4h	E400h	X	--	--	--	SKE	--	--	Skin_ce_mid[1:0]	
Description	**SKE**: Skin Tone Preservation enable control. SKE="0", Skin Tone Preservation disable. SKE="1", Skin Tone Preservation enable. **Skin_ce_mid**: Skin Tone Preservation enable control											
Restriction	--											

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

12.3.2.21 NVMSETE (EAH/EA00H): NVM Address Setting Enable

EAH	NVMSETE (BK0)											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
NVMSETE	W	EAh	EA00h	X	--	--	--	--	--	--	--	ADEN
Description	**ADEN**:NVM Address Setting Enable. ADEN=”0”, NVM Address Setting disable. ADEN=”1”, NVM Address Setting enable.											
Restriction	--											

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

12.3.2.22 CABCCTRL (EEh/EE00h):CABC Control

EEH	CABCCTRL (BK0)										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
CABCCTRL	W	EEh	EE00h	X	--	--	--	LEDPWR SEL	--	--	--	LED ON
Description	**LED_ON**: LED_ON output control LED_ON =”0”,LED_ON output control off. LED_ON =”1”, LED_ON output control on. **LEDPWR SEL**: LED_ON output level selection. LEDPWR SEL =”0”,output level is VDDI. LEDPWR SEL =”1”, output level is VDDB.											
Restriction	--											
Register availability												

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

12.3.2.23 DSTB: Deep Standby Mode Enable

	DSTB										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
PARCTRL	W	FFh	FF00h	X	0	1	1	1	0	1	1	1
	W		FF01h	X	0	0	0	0	0	0	0	1
	W		FF02h	X	0	0	0	0	0	0	0	0
	W		FF03	X	0	0	0	0	0	0	0	0
	W		FF04	X	0	0	0	0	0	0	0	0
	W		FF05		DSTB	0	0	0	0	0	0	0
Description	**DSTB**:DSTB Mode Enable Setting. DSTB=”0”, DSTB Mode Setting disable. DSTB=”1”, DSTB Mode Setting enable.											
Restriction	--											

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

12.3.2.24 DSTBT: Deep Standby Mode Active

	DSTBT										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
PARCTRL	W	FFh	FF00h	X	0	1	1	1	0	1	1	1
	W		FF01h	X	0	0	0	0	0	0	0	1
	W		FF02h	X	0	0	0	0	0	0	0	0
	W		FF03	X	0	0	0	0	0	0	0	0
	W		FF04	X	DSTBT	0	0	0	0	0	0	0
Description	**DSTBT**:DSTB Mode Active. DSTBT="0", DSTB Mode not Active. DSTBT="1", DSTB Mode Active.											
Restriction	--											

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Enter DSTB Mode Flow:

Step1: 0xFF:0x77/0x01/0x00/0x00/0x00/0x80

Step2: 0xFF:0x77/0x01/0x00/0x00/0x80

12.3.3 Command 2 BK1 Function

12.3.3.1 VRHS (B0h/B000h):Vop Amplitude setting

<table>
<tr><td>B0H</td><td colspan="11">VRHS (BK1)</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>VRHS</td><td>W</td><td>B0h</td><td>B000h</td><td>X</td><td colspan="7">VRHA[7:0]</td></tr>
<tr><td>Description</td><td colspan="11">VRHA[7:0]: VRH Set.
Vop=3.5375+(VRHA[7:0]x0.0125);
VRHP=Vop+(Vcom+Vcom offset);
VRHN=-Vop+(Vcom+Vcom offset);</td></tr>
<tr><td>Restriction</td><td colspan="11">--</td></tr>
<tr><td>Register availability</td><td colspan="11">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="11">
<table>
<tr><th>Status</th><th>Default Value (D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>4dh</td></tr>
<tr><td>S/W Reset</td><td>4dh</td></tr>
<tr><td>H/W Reset</td><td>4dh</td></tr>
</table>
</td></tr>
</table>

12.3.3.2 VCOMS (B1h/B100h):VCOM amplitude setting

<table>
<tr><td>B1H</td><td colspan="12">VCOM (BK1)</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>VCOM</td><td>W</td><td>B1h</td><td>B100h</td><td>X</td><td colspan="8">VCOM[7:0]</td></tr>
<tr><td>Description</td><td colspan="12">VCOM[7:0]: VCOM Set.
VCOM=0.1+(VCOM[7:0] x 0.0125);</td></tr>
<tr><td>Restriction</td><td colspan="12">--</td></tr>
<tr><td>Register availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value (D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>40h</td></tr><tr><td>S/W Reset</td><td>40h</td></tr><tr><td>H/W Reset</td><td>40h</td></tr></table></td></tr>
</table>

12.3.3.3 VGHSS (B2h/B200h):VGH Voltage setting

<table>
<tr><td>B2H</td><td colspan="12">VGHSS (BK1)</td></tr>
<tr><td rowspan="2">Inst / Para</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td rowspan="2">D15-8</td><td rowspan="2">D7</td><td rowspan="2">D6</td><td rowspan="2">D5</td><td rowspan="2">D4</td><td rowspan="2">D3</td><td rowspan="2">D2</td><td rowspan="2">D1</td><td rowspan="2">D0</td></tr>
<tr><td>MIPI</td><td>SPI-16</td></tr>
<tr><td>VGHSS</td><td>W</td><td>B2h</td><td>B200h</td><td>X</td><td>--</td><td>--</td><td>--</td><td>--</td><td colspan="5">VGHSS[3:0]</td></tr>
<tr><td>Description</td><td colspan="12">VGHSS[3:0]: Gate High Voltage setting.
<table>
<tr><th>VGHSS[3:0]</th><th>Voltage</th><th>VGHSS[3:0]</th><th>Voltage</th></tr>
<tr><td>00H</td><td>11.5</td><td>07H</td><td>15.0</td></tr>
<tr><td>01H</td><td>12.0</td><td>08H</td><td>15.5</td></tr>
<tr><td>02H</td><td>12.5</td><td>09H</td><td>16.0</td></tr>
<tr><td>03H</td><td>13.0</td><td>0AH</td><td>16.5</td></tr>
<tr><td>04H</td><td>13.5</td><td>0BH</td><td>17.0</td></tr>
<tr><td>05H</td><td>14.0</td><td>0CH</td><td>17.0</td></tr>
<tr><td>06H</td><td>14.5</td><td>0DH</td><td>17.0</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">--</td></tr>
<tr><td>Register availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value (D7 to D0)</th></tr>
<tr><td>Power On Sequence</td><td>02h</td></tr>
<tr><td>S/W Reset</td><td>02h</td></tr>
<tr><td>H/W Reset</td><td>02h</td></tr>
</table></td></tr>
</table>

12.3.3.4 TESTCMD (B3h/B300h):TEST Command Setting

B3H	TESTCMD (BK1)											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
TESTCMD	W	B3h	B300h	X	1	--	--	--	--	0	0	0
Description	**TESTCMD : 0x80H**											
Restriction	--											

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

12.3.3.5 VGLS (B5h/B500h):VGL Voltage setting

B5H	VGLS (BK1)										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
VGLS	W	B5h	B500h	X	--	1	--	--	VGLS[3:0]			

Description

VGLS[3:0]: Gate Low Voltage setting.

VGLS[3:0]	Voltage	VGHSS[3:0]	Voltage
00H	-7.06	08H	-9.83
01H	-7.47	09H	-10.17
02H	-7.91	0AH	-10.53
03H	-8.14	0BH	-10.91
04H	-8.65	0CH	-11.31
05H	-8.92	0DH	-11.74
06H	-9.21	0EH	-12.20
07H	-9.51	0FH	-12.69

Restriction: --

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	07h
S/W Reset	07h
H/W Reset	07h

12.3.3.6 PWCTRL1 (B7h/B700h):Power Control 1

B7H	PWCTRL1 (BK1)										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
PWCTRL1	W	B7h	B700h	X	AP[1:0]		--	--	APIS[1:0]		APOS[1:0]	

Description

AP[1:0]: Gamma OP bias current selection.

AP[1:0]	Current
00H	Off
01H	Min
02H	Middle
03H	Max

APIS[1:0]: Source OP input stage bias current selection

APIS[1:0]	Current
00H	Off
01H	Min
02H	Middle
03H	Max

APOS[1:0]: Source OP output stage bias current selection.

APOS[1:0]	Current
00H	Off
01H	Min
02H	Middle
03H	Max

Restriction: --

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	8Ch
S/W Reset	8Ch
H/W Reset	8Ch

12.3.3.7 PWCTRL2 (B8h/B800h):Power Control 2

B8H	PWCTRL2 (BK1)										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
PWCTRL2	W	B8h	B800h	X	--	--	AVDD[1:0]		--	--	AVCL[1:0]	

Description

AVDD[1:0]: AVDD voltage setting.

AVDD[1:0]	AVDD
00H	6.2 V
01H	6.4 V
02H	6.6 V
03H	6.8 V

AVCL[1:0]: AVCL voltage setting

AVCL[1:0]	AVCL
00H	-4.4 V
01H	-4.6 V
02H	-4.8 V
03H	-5.0 V

Restriction: --

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	21h
S/W Reset	21h
H/W Reset	21h

12.3.3.8 PWCTRL3 (B9h/B900h):Power Control 2

B8H	PWCTRL3 (BK1)										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
PWCTRL3	W	B9h	B900h	X	--	--	SVPO_PUM[1:0]		--	--	SVNO_PUM[1:0]	

Description

SVPO_PUM: source pumping cell setting.

SVPO_PUM[1:0]	Cell set
00H	4
01H	5
02H	6
03H	7

SVNO_PUM: source pumping cell setting.

SVNO_PUM[1:0]	Cell set
00H	4
01H	5
02H	6
03H	7

Restriction: --

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	21h
S/W Reset	21h
H/W Reset	21h

12.3.3.9 PCLKS1 (BAh/BA00h):Power pumping clk selection 1

BAH	PCLKS1 (BK1)										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
PCLKS1	W	BAh	BA00h	X	--	--	STP4CKS[1:0]		--	--	STP1CKS [1:0]	

Description

STP4CKS[1:0]: step4 pumping clk selection.

STP4CKS[1:0]	CLK
00H	3.3 MHz
01H	4.0 MHz
02H	2.5 MHz
03H	6.0 MHz

STP1CKS[1:0]: step1 pumping clk selection.

STP1CKS[1:0]	CLK
00H	3.3 MHz
01H	4.0 MHz
02H	2.5 MHz
03H	6.0 MHz

Restriction: --

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	22h
S/W Reset	22h
H/W Reset	22h

12.3.3.10 PCLKS2 (BBh/BB00h):Power pumping clk selection 2

BBH	PCLKS2 (BK1)										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
PCLKS1	W	BBh	BB00h	X	--	--	--	--	--	--	SBSTCKS[1:0]	

Description

SBSTCKS[1:0]: source pumping clk selection.

SBSTCKS[1:0]	CLK
00H	5.0 MHz
01H	6.7 MHz
02H	8.0 MHz
03H	10 MHz

Restriction: --

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	02h
S/W Reset	02h
H/W Reset	02h

12.3.3.11 PCLKS3 (BCh/BC00h):Power pumping clk selection 3

BCH	PCLKS3 (BK1)										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
PCLKS3	W	BCh	BC00h	X	--	--	STP3CKS[1:0]		STP2CKS[1:0]		STP2SCKS [1:0]	

Description

STP3CKS[1:0]: step3 pumping clk selection.

STP4CKS[1:0]	CLK
00H	2.5 MHz
01H	3.3 MHz
02H	4.0 MHz
03H	5.0 MHz

STP2CKS[1:0]: step2 VGHP pumping clk selection.

STP1CKS[1:0]	CLK
00H	2.5 MHz
01H	3.3 MHz
02H	4.0 MHz
03H	5.0 MHz

STP2SCKS[1:0]: step2 VGHS pumping clk selection.

STP2SCKS[1:0]	CLK
00H	2.5 MHz
01H	3.3 MHz
02H	4.0 MHz
03H	5.0 MHz

Restriction: --

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	22h
S/W Reset	22h
H/W Reset	22h

12.3.3.12 SPD1 (C1h/C100h): Source pre_drive timing set1

C1H	SPD1(BK1)										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
SPD1	W	C1h	C100h	X	0	1	1	1	T2D [3:0]			
Description	**T2D [3:0]:** source pre_drive timing setting.(GND to VDD) Adjust Range : 0 ~ 3 uS 1 step is 0.2uS											
Restriction	--											

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	75h
S/W Reset	75h
H/W Reset	75h

12.3.3.13 SPD2 (C2h/C200h):Source EQ2 Setting

C1H	SPD2 (BK1)										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
SPD2	W	C2h	C200h	X	0	1	1	1	T3D [3:0]			
Description	**T3D [3:0]:** source pre_drive timing setting (VDD to 2*VDD level) Adjust Range : 4 ~ 12 uS 1 step is 0.8 uS											
Restriction	--											
Register availability												
Default												

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value (D7 to D0)
Power On Sequence	75h
S/W Reset	75h
H/W Reset	75h

12.3.3.14 MIPISET1 (D0h/D000h):MIPI Setting 1

D0H	MIPISET1 (BK1)										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
MIPISET1	W	D0h	D000h	X	1	0	0	0	EOT_EN	0	ERR_SEL[1:0]	

Description

EOT_EN: protocol selection error reporting enable

EOT_EN=”0”,disable eotp report error.

EOT_EN=”1”,enable eotp report error.

ERR_SEL[1:0]: ERR pin output signal setting.

ERR_SEL[1:0]	output
00H	Disable
01H	CRC error only
02H	ECC error only
03H	CRC+ECC error

Restriction: --

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

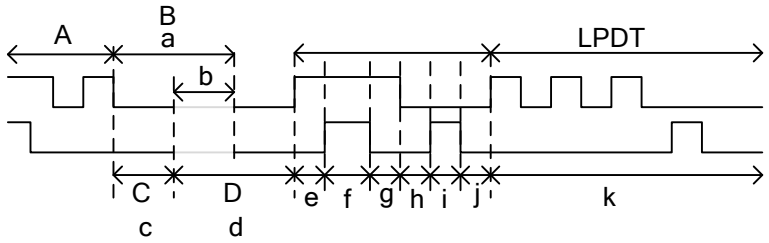
Status	Default Value (D7 to D0)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

12.3.3.15 MIPISET2 (D1h/D100h):MIPI Setting 2

D1H	MIPISET2 (BK1)											
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
MIPISET2	W	D1h	D100h	X	Mpc_tlpx1[3:0]				Mpc_tlpx0{3:0}			
			D101h	X	Mpc_txtimeadj[3:0]				Mpc_tlpx2{3:0}			
			D102h	X	--	--	--	--	Mpc_ttago[3:0]			
			D103h	X	--	--	--	--	Mpc_ttaget[3:0]			

Description

A:Host to Display BTA
B:T_{TA-GO} :Time to drive LP_00 after Turnaround Request
C:$T_{TA-SURE:}$Time-out before new Tx side start driving
D:T_{TA-GET} :Time to drive LP_00 by new Tx



a:Mpc_ttago
b:overlap
c:PHY_ttasure
d:Mpc_ttaget
e:Mpc_tlpx0
f:Mpc_tlpx2
g:Mpc_tlpx0
h:Mpc_tlpx1
i:Mpc_tlpx0
j:Mpc_tlpx1
k:Mpc_txtimeadj

REG	Description	Value
Mpc_tlpx0	Rx LPM state timeout signal	step:
Mpc_tlpx1	Rx LPM state timeout signal	step:
Mpc_tlpx2	RX_to_TX LP11	step:
Mpc_txtimeadj	LPM transmitting time	step:
Mpc_ttago	Tx->Rx BTA timeout signal	Range:0~13, if >13➔13
Mpc_ttaget	Tx BTA setting timeout signal	step:

Restriction: --

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

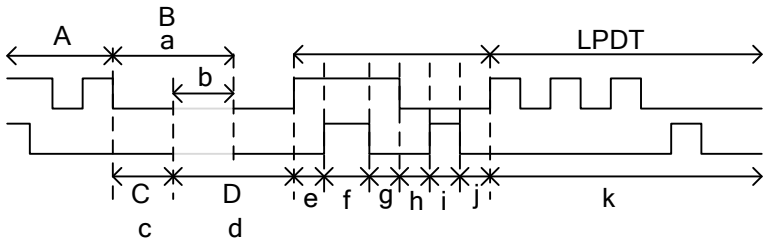
Status	Default Value (D7 to D0)
Power On Sequence	31h/03h/04h/05h
S/W Reset	00h/03h/04h/05h
H/W Reset	00h/03h/04h/05h

12.3.3.16 MIPISET3 (D2h/D200h):MIPI Setting 3

D2H	MIPISET3 (BK1)										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
MIPISET3	W	D2h	D200h	X	--	--	1	1	Phy_ttasure[3:0]			

Description

A:Host to Display BTA
B:T_{TA-GO} :Time to drive LP_00 after Turnaround Request
C:$T_{TA-SURE}$:Time-out before new Tx side start driving
D:T_{TA-GET} :Time to drive LP_00 by new Tx



a:Mpc_ttago
b:overlap
c:PHY_ttasure
d:Mpc_ttaget
e:Mpc_tlpx0
f:Mpc_tlpx2
g:Mpc_tlpx0
h:Mpc_tlpx1
i:Mpc_tlpx0
j:Mpc_tlpx1
k:Mpc_txtimeadj

Phy_ttausre: Rx->Tx BTA timeout signal

Step:

Restriction: --

Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	31h
S/W Reset	31h
H/W Reset	31h

12.3.3.17 MIPISET4 (D3h/D300h):MIPI Setting 4

D3H	MIPISET4 (BK1)										
Inst / Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0
		MIPI	SPI-16									
MIPISET4	W	D3h	D300h	X	--	--	--	1	--	PHY_CSK[2:0]		
			D301h	X		PHY_dsk1[2:0]			--	PHY_dsk0[2:0]		
Description	**PHY_CSK:** MIPI Clock Lane Delay Step: 1 step 200ps **PHY_dsk1:** MIPI Data 1 Lane Delay Step: 1 step 200ps **PHY_dsk0:** MIPI Data 0 Lane Delay Step: 1 step 200ps											
Restriction	--											

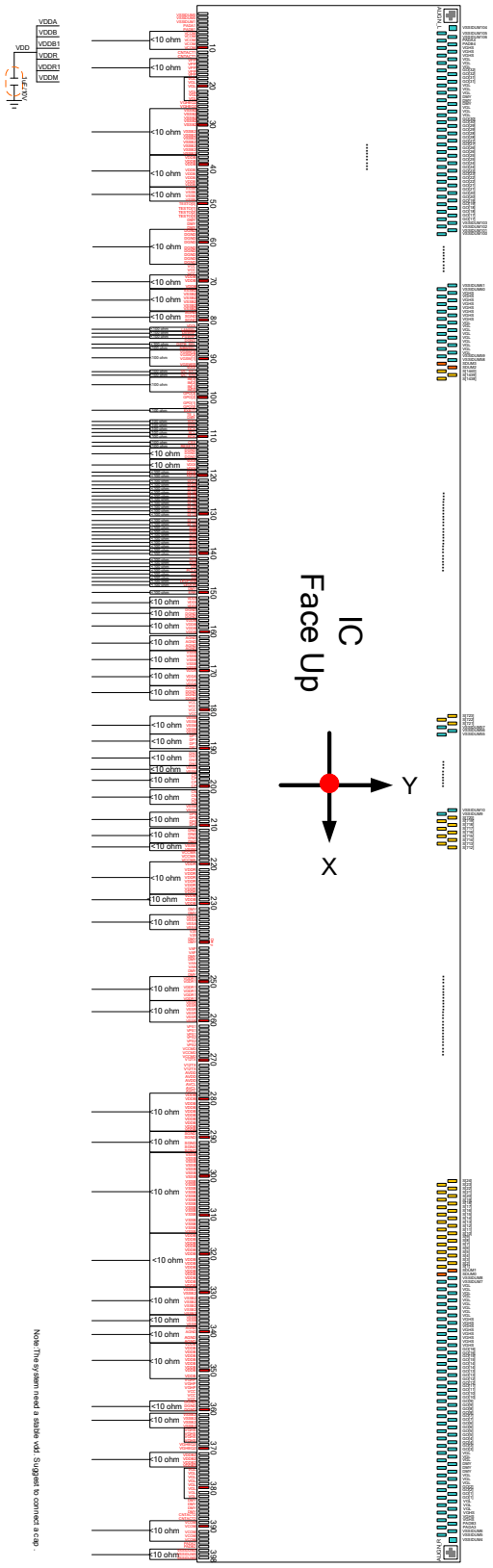
Register availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (D7 to D0)
Power On Sequence	00h/00h
S/W Reset	00h/00h
H/W Reset	00h/00h

13 APPLICATION CIRCUIT



13.1 Voltage Generation

The following is the ST7701S analog voltage pattern diagram:

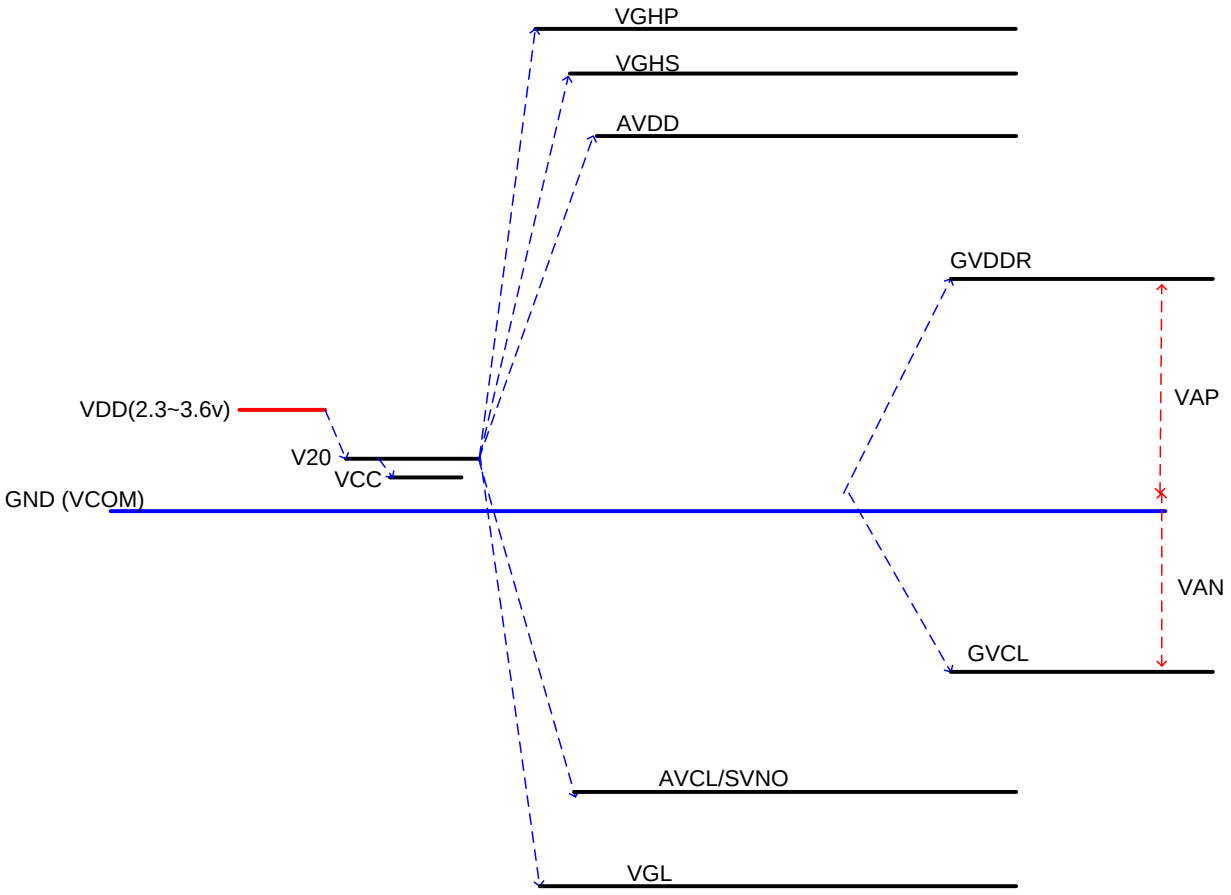


Figure 90 Power Booster Level

13.2 Relationship about source voltage

The relationship about source voltage is shown as below:

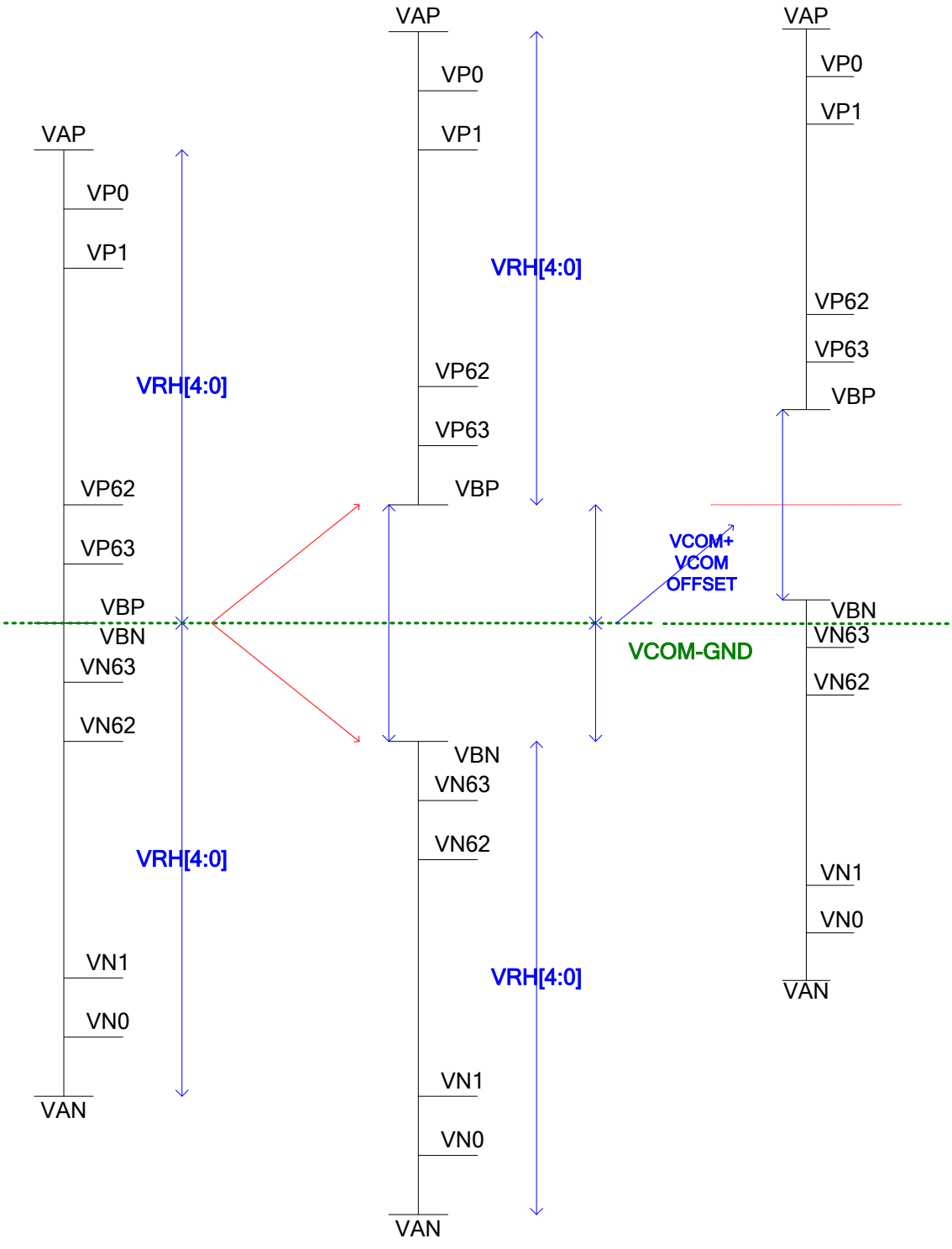


Figure 91 Relationship about source voltage

14 REVISION HISTORY

Version	Date	Description
V1.0	2017/03	Release Version
V 1.1	2017/04	1、 pad name (p14~34) 2、 A1 read Value (p247)